Enrolment No/Seat No.: _____

R.N.G.PATEL INSTITUTE OF TECHNOLOGY-RNGPIT

(An Autonomous Institute U/s UGC Act 1956)

B.Tech. SEMESTER-II, SEMESTER END EXAMINATION – WINTER 2025

SUBJECT CODE: 1EL202 **DATE: 08-01-2026**

SUBJECT NAME: DIGITAL LOGIC DESIGN

TIME: 11:00 AM to 01:30 PM **TOTAL MARKS: 70**

Instructions

1. It is **compulsory** for students to write **Enrolment No. /Seat No.**on the question paper.
2. Write answers of**Section A** and **Section B** in **separate answer books**.
3. Attempt all questions from both **Section A** and **Section B**.
4. Each section carries **35 marks**, with a total of **70 marks** for the examination.
5. The figures to the right of each question indicate full marks, make suitable assumptions with justification.
6. BL - Bloom's Taxonomy Levels (R-Remember, U-Understanding, A –Application, N –Analyze, E – Evaluate, C -Create), CO - Course Outcomes.

SECTION A

		Marks	BL	CO
Q.1	**Multiple-Choice Questions**	**[05]**		
(a)	Universal gates are:	**1**	**R**	**1**
	(i) AND & OR **(ii)** XOR & XNOR			
	(iii) NAND & NOR **(iv)** NOT & AND			
(b)	A 3-to-8 decoder has how many outputs?	**1**	**R**	**2**
	(i) 3 **(ii)** 7			
	(iii) 8 **(iv)** 2			
(c)	In a half adder, carry is produced when:	**1**	**U**	**2**
	(i) Both inputs are 0 **(ii)** Both inputs are 1			
	(iii) Inputs are different **(iv)** Inputs are same			
(d)	Memory elements in sequential circuits are usually:	**1**	**U**	**3**
	(i) Logic gates **(ii)** Flip-flops			
	(iii) Decoders **(iv)** Multiplexers			

(e) A D flip-flop is also called a:		**1**	**R**	**3**
(i) Delay flip-flop **(ii)** Data flip-flop **(iii)** Both (i) & (ii) **(iv)** None of the above				
Q.2 Attempt Any Two		**[10]**		
(a) Prove De-Morgan's theorem.		**5**	**E**	**1**
(b) Converts from one number system to another number system: (i) $(1018)_{10} = (\_\_\_\_\_)_2$ (ii) $(275)_8 = (\_\_\_\_\_)_{10}$ (iii) $(FFF)_{16} = (\_\_\_\_\_)_2$		**5**	**A**	**1**
(c) Compare Digital logic families.		**5**	**E**	**1**
Q.3 Attempt Any Two		**[10]**		
(a) Simplify the following Boolean expressions and realize using AOI gates. $Y = \Sigma m\ (0,2,8,9,10,12,13,14)$		**5**	**N**	**2**
(b) Explain full Subtractor.		**5**	**U**	**2**
(c) Explain BCD to Excess 3 code converter.		**5**	**U**	**2**
Q.4 Attempt Any Two		**[10]**		
(a) Explain S-R flip-flop.		**5**	**U**	**3**
(b) Explain the Serial In Serial Out (SISO) shift register.		**5**	**U**	**3**
(c) Explain 3 – bit Synchronous Up Counter.		**5**	**A**	**3**

SECTION B

	Marks	BL	CO
Q.5 Multiple-Choice Questions	**[05]**		
(a) In D to A converter , the smallest change in analog output voltage for one bit change in digital input is called the	**1**	**R**	**4**
(i) Quantization error **(ii)** Resolution			
(iii) Accuracy **(iv)** Signal to noise ratio			
(b) The Successive Approximation Register A/D converter works on principle of	**1**	**U**	**4**
(i) Binary Search Algorithm **(ii)** Current to voltage converter			
(iii) Voltage to current converter **(iv)** Counter			
(c) Quantization error in ADC is	**1**	**E**	**4**
(i) ± LSB **(ii)** ± (0.25) LSB			
(iii) ± (0.5) LSB **(iv)** ± (0.75) LSB			
(d) Nyquist Theorem states (if Fs = sampling frequency and Fmax = maximum input frequency)	**1**	**E**	**4**
(i) 0.5 Fs = 1.5 Fmax **(ii)** Fs = Fmax			
(iii) 1.5 Fmax = 0.5 Fs **(iv)** 3 Fs = 6 Fmax			
(e) A 8K × 8 semiconductor memory chip can store how many bytes of data?	**1**	**N**	**5**
(i) 8192 bytes **(ii)** 64000 bytes			
(iii) 80 bytes **(iv)** 64 bytes			
Q.6 Attempt Any Two	**[10]**		
(a) What is R-2R Ladder type D/A converter? Explain with complete circuits and example.	**5**	**A**	**4**
(b) What is the basic concept of parallel comparator A/D converter? Draw and explain 3-bit parallel comparator A/D converter with necessary circuit diagram and output stages.	**5**	**E**	**4**
(c) Explain basic key process in detail : Sampling , quantization and codding in signal converter	**5**	**U**	**4**
Q.7 Attempt Any Two	**[10]**		
(a) What is the need for memory expansion? List out common methods for memory expansion.	**5**	**R**	**5**

(b) What are SPLDs, CPLDs, and FPGAs? Explain in detail	**5**	**U**	**5**
(c) Compare: Programmable logic array (PLA), Programmable array logic (PAL).	**5**	**N**	**5**

Q.8 Attempt Any Two **[10]**

(a) What is memory? Give classification and characteristic of memory.	**5**	**R**	**5**
(b) Write a short note on : successive approximation A/D converter	**5**	**A**	**4**
(c) What is sample and hold circuit? How it works? Explain it in detail	**5**	**A**	**4**

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