

R.N.G.PATEL INSTITUTE OF TECHNOLOGY-RNGPIT
(An Autonomous Institute U/s UGC Act 1956)

B.Tech. SEMESTER-III, SEMESTER END EXAMINATION – WINTER 2025

SUBJECT CODE: 1CS305

DATE: 26-12-2025

**SUBJECT NAME: COMPUTER ORGANIZATION AND
ARCHITECTURE**

TIME: 11:00 AM to 01:30 PM

TOTAL MARKS: 70

Instructions

1. It is **compulsory** for students to write **Enrolment No. /Seat No.** on the question paper.
2. Write answers of **Section A** and **Section B** in **separate answer books**.
3. Attempt all questions from both **Section A** and **Section B**.
4. Each section carries **35 marks**, with a total of **70 marks** for the examination.
5. The figures to the right of each question indicate full marks, make suitable assumptions with justification.
6. BL - Cognitive Level (As per Revised Bloom's Taxonomy) (R-Remember, U-Understanding, A –Application, N –Analyze, E – Evaluate, C -Create), CO - Course Outcomes.

SECTION A

		Marks	BL	CO
Q.1	(a) Write an Assembly level program for addition of 50 numbers.	03	N	2
	(b) Draw the flowchart of first pass of the assembler and explain working of the same.	04	A	2
Q.2	(a) Define Register Transfer Language (RTL) with example.	03	R	1
	(b) Explain the computer registers used in a basic computer with block diagram.	04	A	1
	(c) Explain the concept of common bus organization in a computer with neat and clean diagram.	07	U	1
OR				
Q.2	(a) Define Accumulator Register and write a short note on the same.	03	R	1
	(b) Construct diagram of common bus system of four 4-bits registers with diagram.	04	A	1
	(c) Explain the instruction cycle in detail with flowchart.	07	U	1
Q.3	(a) Define pipelining. What are its advantages?	03	R	4
	(b) Compare RISC and CISC architecture.	04	N	4
	(c) Elaborate Flynn's classification scheme with proper diagram.	07	U	4

OR

Q.3	(a) Explain floating point arithmetic operations: addition, subtraction-with examples.	03	R	4
	(b) Explain the difference between static and dynamic pipelines.	04	N	4
	(c) Describe the Booth multiplication algorithm with an example.	07	U	4

SECTION B

		Marks	BL	CO
Q.4	(a) Explain cache coherence problem.	03	U	6
	(b) Illustrate with a block diagram how a crossbar switch is implemented in multiprocessor systems.	04	A	6
Q.5	(a) In zero-address instructions format, how data from memory is accessed? Explain with example.	03	U	3
	(b) Compare: RISC and CISC.	04	N	3
	(c) What is register stack? Explain push and pop micro-operations.	07	U	3

OR

Q.5	(a) What is Interrupt? Explain types of interrupt.	03	U	3
	(b) Differentiate between hardwired control unit and micro programmed control unit.	04	N	3
	(c) What is meant by addressing modes? Explain any five addressing modes by taking proper example.	07	U	3
Q.6	(a) Explain Interrupt initiated I/O.	03	U	5
	(b) Explain the working of Direct Memory Access (DMA).	04	U	5
	(c) Demonstrate with an example how Content Addressable Memory (CAM) can be implemented to speed up memory access in computer architecture.	07	A	5

OR

Q.6	(a) Briefly explain source initiated transfer using handshaking.	03	U	5
	(b) Explain daisy chain priority interrupt.	04	U	5
	(c) Demonstrate the process of mapping memory addresses into cache lines using set-associative mapping for a given set of addresses.	07	A	5
