Enrolment No/Seat No.: _____

R.N.G.PATEL INSTITUTE OF TECHNOLOGY-RNGPIT

(An Autonomous College U/s UGC Act 1956)

B. Tech. SEMESTER-II, SEMESTER END EXAMINATION –SUMMER 2025

Subject Code: 1EL202 **Date: 23-05-2025**

Subject Name: DIGITAL LOGIC DESIGN

Time: 11:00 AM to 01:30 PM **Total Marks: 70**

Instructions

1. It is **compulsory** for students to write **Enrolment No. /Seat No.**on the question paper.
2. Write answers of**Section A** and **Section B** in **separate answer books**.
3. Attempt all questions from both **Section A** and **Section B**.
4. Each section carries **35 marks**, with a total of **70 marks** for the examination.
5. The figures to the right of each question indicate full marks, make suitable assumptions with justification.
6. BL - Bloom's Taxonomy Levels (R-Remember, U-Understanding, A –Application, N –Analyze, E – Evaluate, C -Create), CO - Course Outcomes.

SECTION A

		Marks	BL	CO
Q.1	**Multiple-Choice Questions**	**[05]**		
(a)	What is the output if both inputs of an EX-NOR gate are at the opposite logic level?	**1**	**R**	**1**
	(i) 1 **(ii)** 0			
	(iii) No output **(iv)** Either 0 or 1			
(b)	If A=1 & B=1 is the input in half adder then output will be	**1**	**R**	**2**
	(i) Sum=1 Carry=1 **(ii)** Sum=1 Carry=0			
	(iii) Sum=0 Carry=1 **(iv)**Sum=0 Carry=0			
(c)	Number of select lines for 16 X 1 Multiplexer are	**1**	**A**	**2**
	(i) 2 **(ii)**4			
	(iii) 3 **(iv)** 5			
(d)	The fastest type of analog-to-digital converter is	**1**	**R**	**4**
	(i) Successive Approximation type **(ii)** Counter type			
	(iii) Flash type **(iv)** None of above			

(e)	In a J-K flip-flop, if J=K=1 the resulting flip-flop is referred to as	**1**	**U**	**3**
	(i) D flip-flop **(ii)** S-R flip-flop			
	(iii) T flip-flop **(iv)** S-K flip-flop			

Q.2 Attempt Any Two **[10]**

(a)	Draw the logic symbol, write Boolean expression and construct the truth table for following logic gates. (1) AND GATE (2) OR GATE (3) NAND GATE (4) EX-OR GATE (5) NOR GATE.	**5**	**R**	**1**
(b)	Converts from one number system to another number system. (1) $(112)_{10} = (?)_2$ (2) $(11001011)_2 = (?)_8$ (3) $(1001011)_2 = (?)_{10}$ (4) $(111100111011)_2 = (?)_{16}$ (5) $(32)_{10} = (?)_2$	**5**	**A**	**1**
(c)	Explain following logic family: 1. TTL 2. CMOS	**5**	**R**	**1**

Q.3 Attempt Any Two **[10]**

(a)	State & Explain Simplify the following expression and draw circuit for the output $Y = \Sigma m\,(1,3,4,6,8,9,11,12,13,15) + d(0,5,7)$	**5**	**R**	**2**
(b)	Design & Explain 4 bit Binary to Gray code converter.	**5**	**A**	**2**
(c)	Explain Full adder using two half adders.	**5**	**A**	**2**

Q.4 Attempt Any Two **[10]**

(a)	Differentiate between combinational logic circuit and sequential logic circuit.	**5**	**R**	**3**
(b)	Explain J-K Flip Flop with its circuit diagram, truth table and excitation table.	**5**	**U**	**3**
(c)	Design Mod-6 Asynchronous counter using T FFs.	**5**	**A**	**3**

SECTION B

		Marks	BL	CO
Q.5	**Multiple-Choice Questions**	**[05]**		
(a)	Determine the resolution of a 6-bit DAC in terms of percentage: **(i)** 15.87% **(ii)** 0.158% **(iii)** 1.587% **(iv)** 1.687%	**1**	**A**	**4**
(b)	Which type of memory loses its stored data when the power supply is removed? **(i)** ROM **(ii)** PROM **(iii)** EEPROM **(iv)** RAM	**1**	**R**	**5**
(c)	An R-2R ladder DAC utilizes only two resistor values, R and 2R, which helps in achieving better: **(i)** Conversion speed **(ii)** Power efficiency **(iii)** Accuracy and ease of fabrication **(iv)** Output current range	**1**	**U**	**4**
(d)	Which of the following is a key characteristic of Field Programmable Gate Arrays (FPGAs)? **(i)** Fixed logic functionality after manufacturing. **(ii)** One-time programmable logic. **(iii)** Reconfigurable hardware architecture after manufacturing. **(iv)** Limited to implementing only combinational logic.	**1**	**R**	**5**
(e)	Expanding the memory size of a system by increasing the number of address lines allows for: **(i)** Storing more bits per memory location **(ii)** Accessing data faster **(iii)** Addressing a larger number of memory locations **(iv)** Reducing power consumption.	**1**	**U**	**5**
Q.6	**Attempt Any Two**	**[10]**		
(a)	Define the following parameters of DACs: (i) Accuracy, (ii) Settling time, (iii) Resolution, (iv) Offset Voltage, (v) Monotonicity	**5**	**R**	**4**

(b)	The Logic levels used in a 4-bit R-2R ladder DAC are: Logic 1 = 5 V and Logic 0 = 0 V. Find the output voltage for inputs (i) 0101, (ii) 1011, and (iii) 1010.	**5**	**A**	**4**
(c)	Explain Successive Approximation ADC with neat diagram	**5**	**U**	**4**

Q.7 Attempt Any Two **[10]**

(a)	Explain the Weighted Register type DAC. Discuss the advantages and disadvantages of this type of DAC. Also calculate output voltage for input 1101 for 4-bit Weighted Register type DAC if V_{ref} = 5 V, R_f = 500 Ω and R = 1 KΩ.	**5**	**U**	**4**
(b)	Explain the architecture and working principle of a Programmable Logic Array (PLA). How does it differ from a Programmable Array Logic (PAL)?	**5**	**U**	**5**
(c)	Explain flash-type ADC with neat diagram. If 5-bit flash-type ADC has a reference voltage of 20 V. How many voltage comparators and resistors does it have? What is the increment between the voltages applied to the comparators?	**5**	**A**	**4**

Q.8 Attempt Any Two **[10]**

(a)	Explain the basic architecture of a Field Programmable Gate Array (FPGA). Describe the function of Configurable Logic Blocks (CLBs) and the programmable routing resources within an FPGA.	**5**	**U**	**5**
(b)	Draw a logic diagram showing how to interconnect 2K × 8 memory circuits to obtain 4K × 8 memory? Each circuit has an active-LOW chip select input and common data-in /data-out pins.	**5**	**A**	**5**
(c)	Explain different types of ROMs.	**5**	**U**	**5**