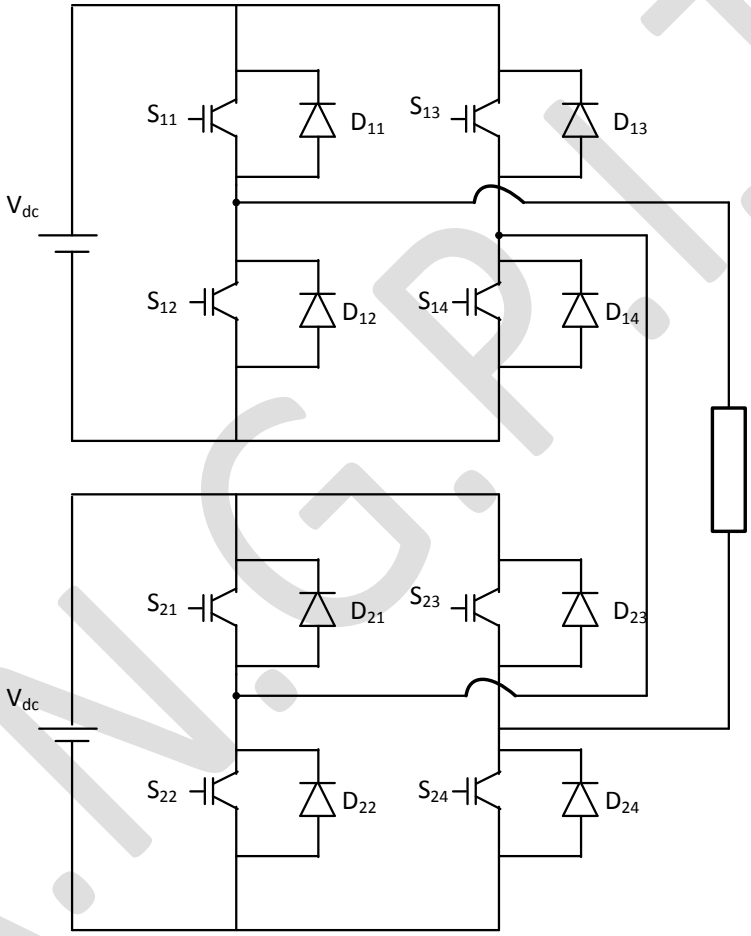
# Class notes : APE,

# Multilevel Inverter Lect:3

## Cascade Multi level Inverter (Symmetrical)




5 Level Cascade Multilevel Inverter

- The output phase level voltage is N=2*Ns*+1; Where Ns is the number of dc source

**Operation:**

- As shown in the figure total 5 level of output voltage can be achieved; i.e. +2Vdc, +Vdc, 0, -Vdc, -2Vdc

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- By switching combination, we can obtain the different level of output voltage, for example when $S_{11}$ and $S_{14}$ switches are ON output voltage of upper inverter is +Vdc and at the same time when $S_{21}$ and $S_{24}$ switches are ON output voltage of lower inverter is also +Vdc, so total output voltage across the load is +2Vdc.
- Table shows the summary of output voltage with different switching states:

(Student Note: In case of switching redundancy, only one switching combinations are shown in the table, remaining possibilities students have to find out and fill the table)

| Vo | $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $S_{21}$ | $S_{22}$ | $S_{23}$ | $S_{24}$ |
|---|---|---|---|---|---|---|---|---|
| 2Vdc | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| Vdc | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| 0 | | | | | | | | |
| | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | | | | | | | |
| | | | | | | | | |
| -Vdc | | | | | | | | |
| | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | | | | | | | |
| | | | | | | | | |
| -2Vdc | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

**Feature:**

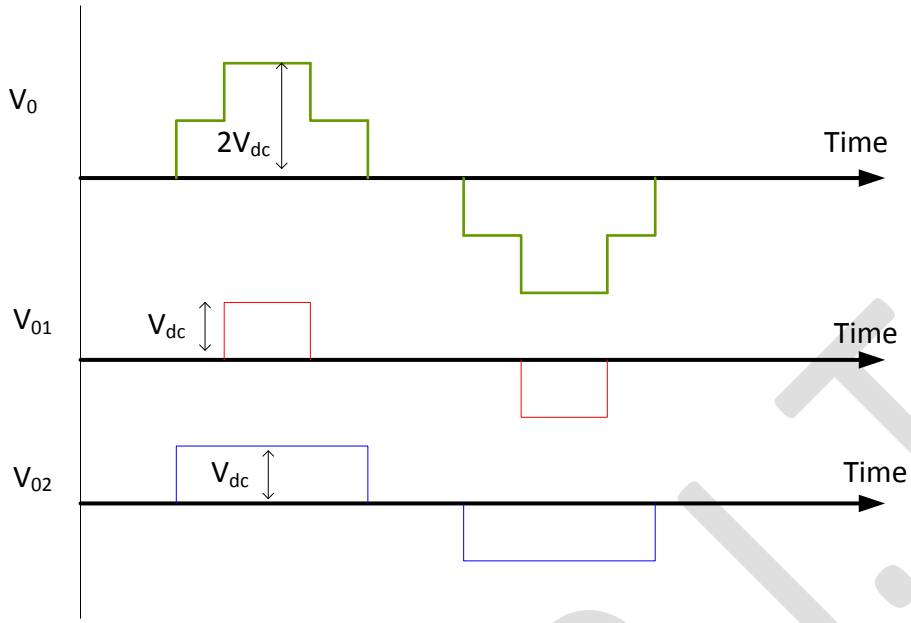
- Need separate DC source (not suitable for AC-DC then DC_AC); well suitable for renewable
- If not switching synchronising, short circuit can be introduced
- All switching devices stress are equal

**Advantages:**

- List no of component requirement to achieve same level
- Optimize circuit layout and packages
- Soft switching can be used to reduce switching losses
- In parallel connection, device shares current, so topology is good for high current loads

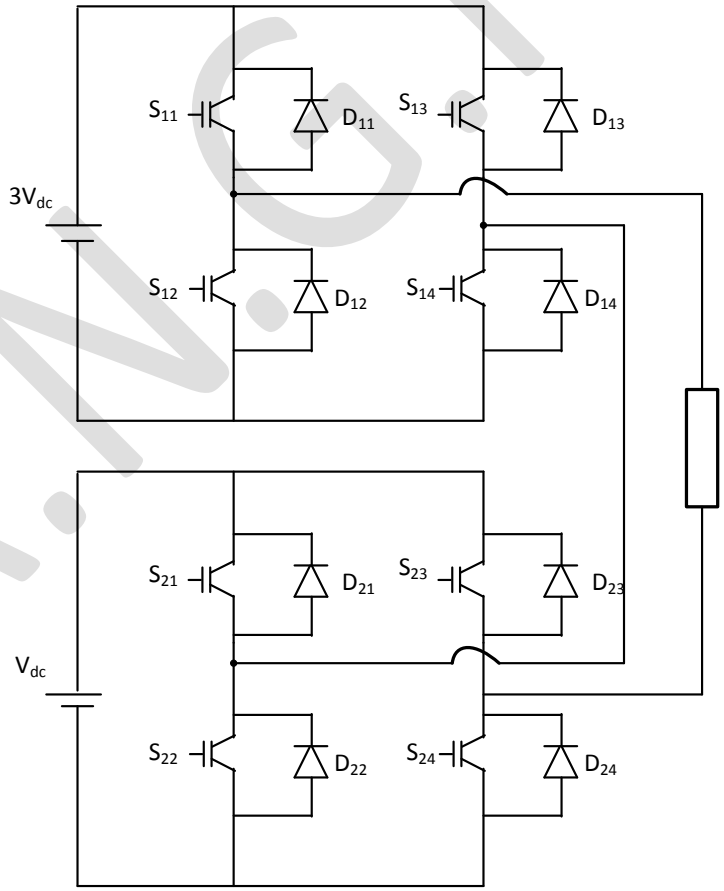
**Disadvantages:**

- Needs separate dc source




Waveforms of 5 level cascade MLI

## Cascade Multi level Inverter (Asymmetrical)



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9 Level Cascade Asymmetrical Multilevel Inverter

- Upper cell switches must have high voltage blocking capabilities
- Generate 9 level of output voltage using only 2 separate dc source
- Use Transformer to provide isolated dc power supply
- HV stage will be supplied more power to the load under this condition LV stage will require to operate in rectification mode



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