Class notes : APE,

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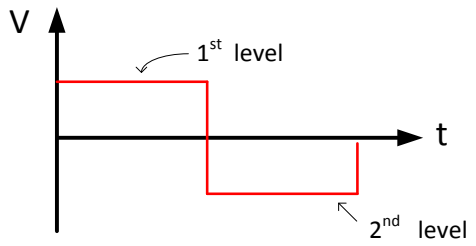
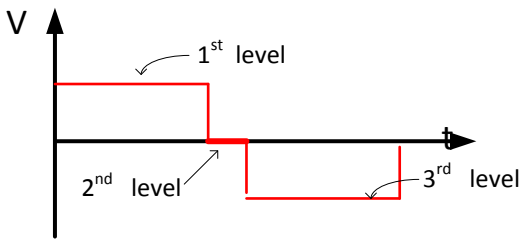
Multilevel Inverter

Definition: The number of steps in the voltage of the output terminal with respect to any arbitrary internal reference point.

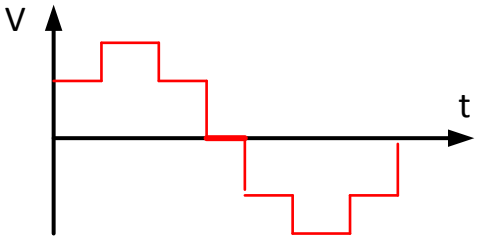
- Generated stepped waveform output voltage with adjusted frequency and amplitude.



2 level Inverter



3 level Inverter



5 level Inverter

Question: Why Multilevel Inverter is required? Or Difference between two level and Multilevel Inverter

2 Level Inverter	Multilevel Inverter
1) The stress on the device is high in case of two level inverter as $\frac{dv}{dt}$ is high in this configuration.	1) The stress on the device is low as voltage increases in stepped manner and so that $\frac{dv}{dt}$ is lower in this type configuration
2) Higher voltage operation is difficult	2) Higher voltage operation is easily

	possible as voltage is distributed among the series connected switches
3) Filter size requirement is higher in two level	3) MLI (Multi level Inverter) reduces the filter size requirement
4) As power level increases, dc link voltage and switching frequency has to be reduced. This action lead to generate lower order harmonics (7^{th} and 9^{th})	4) MLI reduces the lower order harmonics and operates with lower switching frequencies
5) Devise rating is high in case of 2 level inverter	5) Device rating reduces significantly and this will reduces the cost of MLI

Types of MLI:

1) Diode clamped MLI or Neutral Point Clamped (NPC) MLI
2) Flying capacitor type MLI
3) Cascade H-Bridge MLI

Diode Clamped MLI:

Three level Diode Clamped MLI:

- Fig. 1 shows the one leg of Inverter (total three legs of three phase)
- No of Capacitor require= (N-1) =2 ; where N is the level of Inverter
  No of switches required/phase= 2(N-1) =4
  Any times switches 'ON'= (N-1) =2

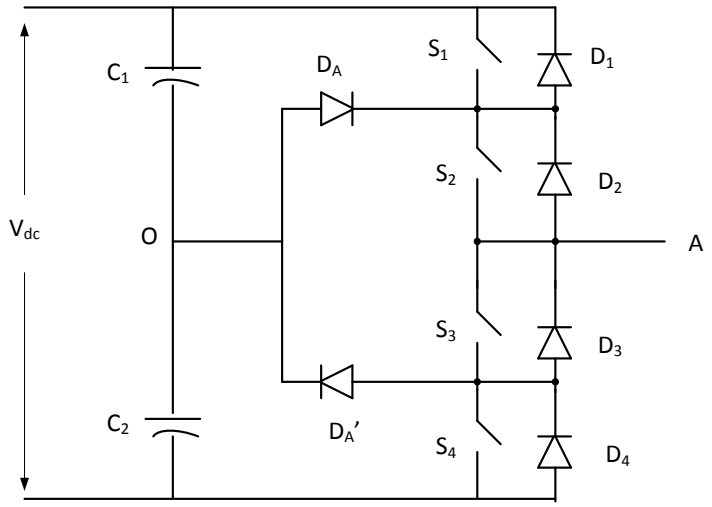
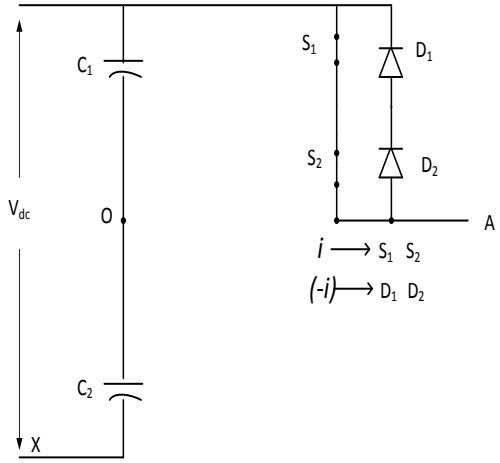


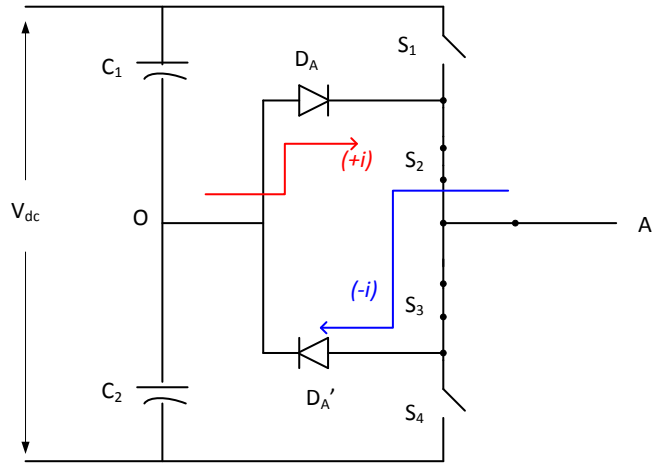
Fig.1: 3-Level Diode clamped MLI

When S1 and S2 are 'ON':



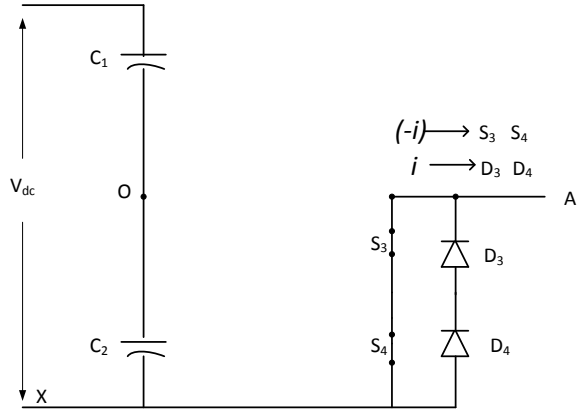
- Here, $V_{ax}=V_{dc}$ and $V_{ao}=V_{dc}/2$;
- The positive direction of current flows through -C_2-C_1 -switch S_1 and S_2
- The negative direction of current (Load to source) flows through diode D_1 and D_2-C_1-C_2

When S_2 and S_3 are 'ON':



- Here, $V_{ax}= V_{dc}/2$and $V_{ao}=0$;
- The positive direction of current flows through -D_A -switch S_2
- The negative direction of current (Load to source) flows through-switch S_3-and D_A'

When S_3 and S_4 are 'ON':



- Here, $V_{ax}=0$ and $V_{ao}= - V_{dc}/2$;
- The positive direction of current flows through -C_1-C_2 -diode D_4 and D_3
- The negative direction of current (Load to source) flows through switch S_3-S_4 and -C_2-C_1

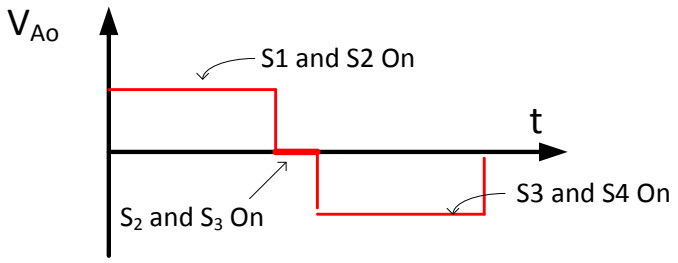


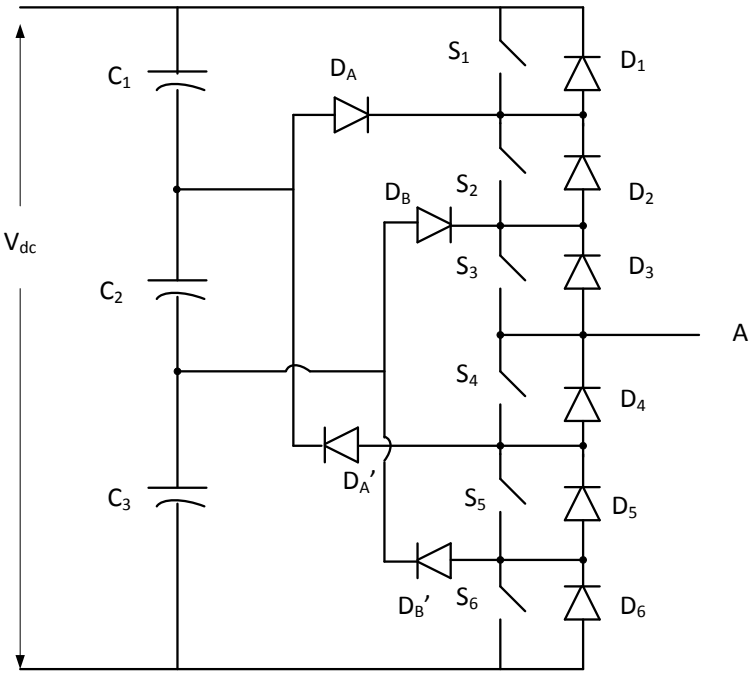
Fig.2: Output Pole Voltage V_{AO}

Switching state of 3 level Inverter:

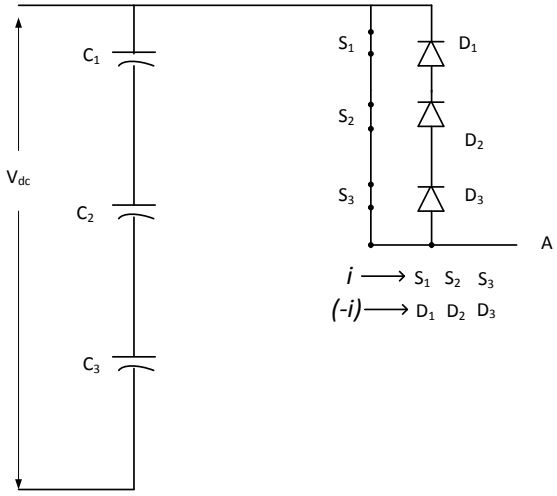
Switching state	S_1	S_2	S_3	S_4	V_{AO}	V_{AX}
	ON	ON	OFF	OFF	$V_{dc}/2$	V_{dc}
	OFF	ON	ON	OFF	0	$V_{dc}/2$
	OFF	OFF	ON	ON	$-V_{dc}/2$	0

Four level Diode Clamped MLI:

- Fig. 4 shows the one leg of Inverter (total three legs of three phase)
- No of Capacitor require= (N-1) =3 ; where N (=4) is the level of Inverter
  No of switches required/phase= 2(N-1) =6
  Any times switches 'ON'= (N-1) =3

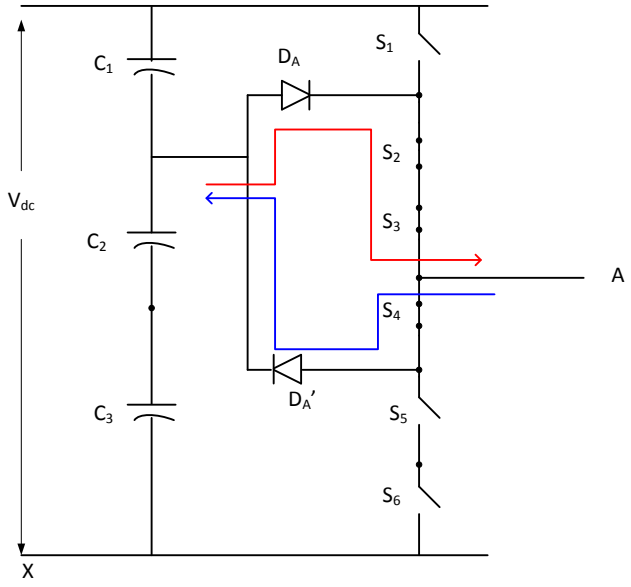


When S_1, S_2 and S_3 are 'ON':



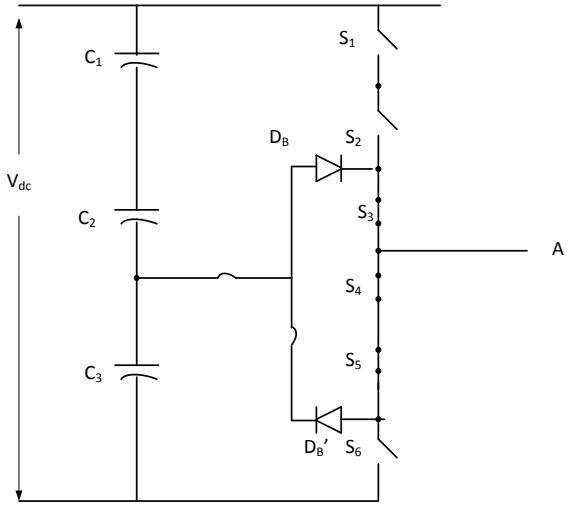
- Here, $V_{ax}=V_{dc}$;
- The positive direction of current flows through C_3-C_2-C_1 -switch S_1 S_2 and S_3
- The negative direction of current (Load to source) flows through diode D_1 D_2 and D_3-C_1-C_2-C_3

When S_2, S_3 and S_4 are 'ON':



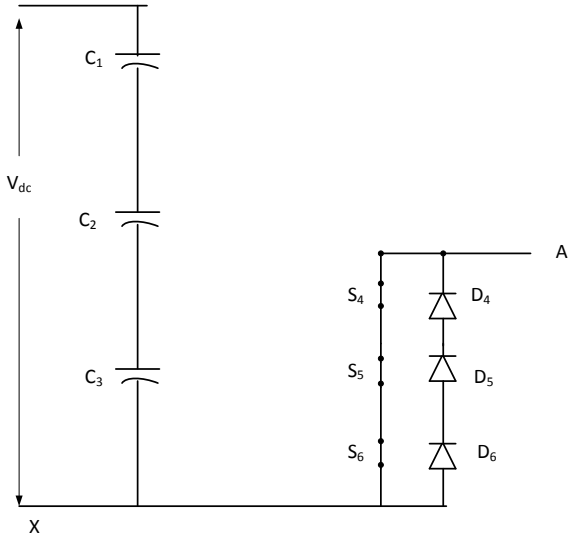
- Here, $V_{ax}=2V_{dc}/3$;
- The positive direction of current flows through D_A –switch S_2 and S_3
- The negative direction of current (Load to source) flows through S_4 diode D_A'

When S_3, S_4 and S_5 are 'ON':



- Here, $V_{ax}=V_{dc}/3$;
- The positive direction of current flows through D_B –switch S_3
- The negative direction of current (Load to source) flows through S_4 S_5diode D_B'

When S_4, S_5 and S_6 are 'ON':



- Here, $V_{ax}=0$;

Features of NPC MLLI (or Diode Clamped MLI):

- In 4 Level NPC MLI D_A has to block 1/3 V_{dc} (Rating)
- D_A' has to block 2/3 V_{dc}
- Separate heat sink required in this case
- Voltage unbalance issue: When o/p voltage is Vdc: C1, C2, C3 supply the power and When o/p voltage is 2/3 Vdc C2, C3 supply the power-> so voltage across C1 increases compare to other two capacitors.

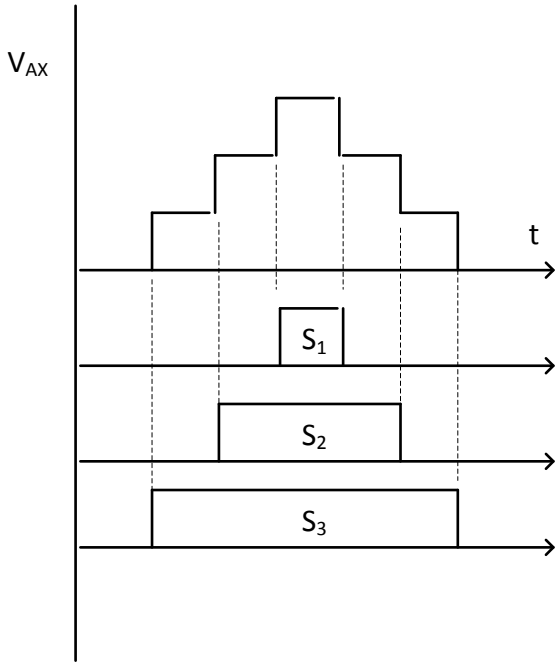


Fig.4: Output Voltage V_{AX}

Advantages:

- Filter size reduces
- All switches operate at fundamental frequency so switching losses are reduced and efficiency increase.
- Control Method is simple

Disadvantage:

- When no of level increases, no of clamping diode increases.