Unit 5: Field effect transistors (FET) and its Biasing

1.1 Introduction

- The bipolar junction transistor (BJT) relies on two types of charge: free electrons and holes. This is why it is called bipolar: the prefix bi stands for “two.”
- This chapter discusses another kind of transistor called the field-effect transistor (FET). This type of device is unipolar because its operation depends on only one type of charge, either free electrons or holes.
- In other words, an FET has majority carriers but not minority carriers. For most linear applications, the BJT is the preferred device.
- But there are some linear applications in which the FET is better suited because of its high input impedance and other properties. Furthermore, the FET is the preferred device for most switching applications. Why?
- Because there are no minority carriers in an FET. As a result, it can switch off faster since no stored charge has to be removed from the junction area.
- There are two kinds of unipolar transistors: JFETs and MOSFETs. The first part of this chapter discusses the junction field- effect transistor (JFET) and its applications. In later part, we discuss the metal-oxide semiconductor FET (MOSFET) and its applications.

1.2 Basic Ideas

- Figure-1a shows a piece of n-type semiconductor. The lower end is called the source, and the upper end is called the drain. The supply voltage V_{DD} forces free electrons to flow from the source to the drain.

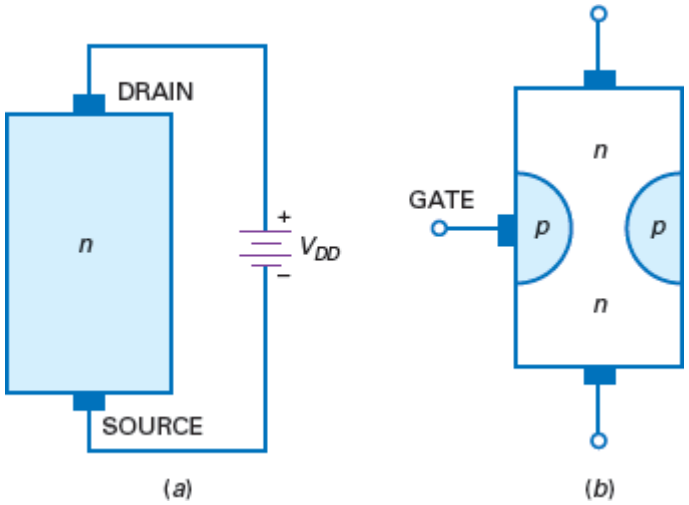


Figure-1 (a) Part of JFET; (b) single-gate JFET

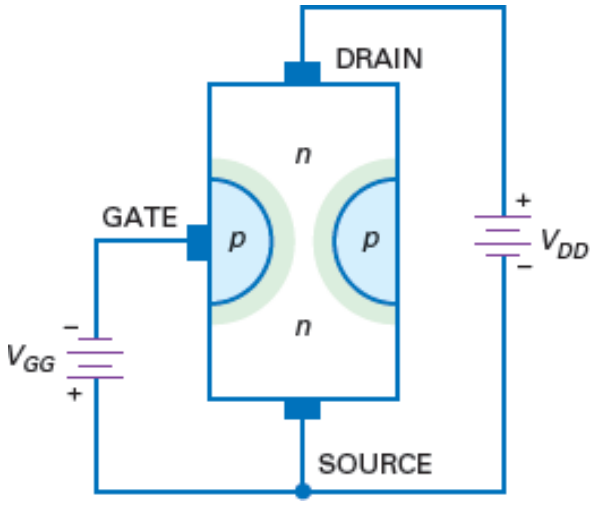
- To produce a JFET, a manufacturer diffuses two areas of p-type semiconductor into the n-type semiconductor, as shown in Figure-1b. These p regions are connected internally to get a single external gate lead.

1.2.1 Field Effect

- Figure-2 shows the normal biasing voltages for a JFET. The drain supply voltage is positive, and

the gate supply voltage is negative.

The term field effect is related to the depletion layers around each p region. These depletion layers exist because free electrons diffuse from the n regions into the p regions. The recombination of free electrons and holes creates the depletion layers shown by the colored areas.



1.2.2 Reverse Bias of Gate

- In Figure-2, the p-type gate and the n-type source form the gate-source diode. With a JFET, we always reverse-bias the gate-source diode.
- Because of reverse bias, the gate current I_G is approximately zero, which is equivalent to saying that the JFET has an almost infinite input resistance.
- A typical JFET has an input resistance in the hundreds of mega-ohms. This is the big advantage that a JFET has over a bipolar transistor. It is the reason that JFETs excel in applications in which a high input impedance is required.
- One of the most important applications of the JFET is the source follower, a circuit like the emitter follower, except that the input impedance is in the hundreds of mega-ohms for lower frequencies.

1.2.3 Gate Voltage Controls Drain Current

- In Figure-2, electrons flowing from the source to the drain must pass through the narrow channel between the depletion layers. When the gate voltage becomes more negative, the depletion layers expand and the conducting channel becomes narrower. The more negative the gate voltage, the smaller the current between the source and the drain.
- The JFET is a voltage-controlled device because an input voltage controls an output current. In a JFET, the gate-to-source voltage V_{GS} determines how much current flows between the source and the drain.
- When V_{GS} is zero, maximum drain current flows through the JFET. This is why a JFET is referred to as a normally on device. On the other hand, if V_{GS} is negative enough, the depletion layers touch and the drain current is cut off.

1.2.4 Schematic Symbol

- The JFET of Figure-2 is an n-channel JFET because the channel between the source and the drain is an n-type semiconductor. Figure-3a shows the schematic symbol for an n-channel JFET. In many low-frequency applications, the source and the drain are interchangeable because you can use either end as the source or the other end as the drain.
- The source and drain terminals are not interchangeable at high frequencies. Almost always, the manufacturer minimizes the internal capacitance on the drain side of the JFET.
- In other words, the capacitance between the gate and the drain is smaller than the capacitance between the gate and the source. You will learn more about internal capacitances and their effect on circuit action in a later chapter.
- Figure-3b shows an alternative symbol for an n-channel JFET. This symbol with its offset gate is preferred by many engineers and technicians. The offset gate points to the source end of the device, a definite advantage in complicated multistage circuits.
- There is also a p-channel JFET. The schematic symbol for a p-channel JFET, shown in Figure-3c, is similar to that for the n-channel JFET, except that the gate arrow points in the opposite direction.
- The action of a p-channel JFET is complementary; that is, all voltages and currents are reversed. To reverse-bias a p-channel JFET, the gate is made positive in respect to the source. Therefore, V_{GS} is made positive.

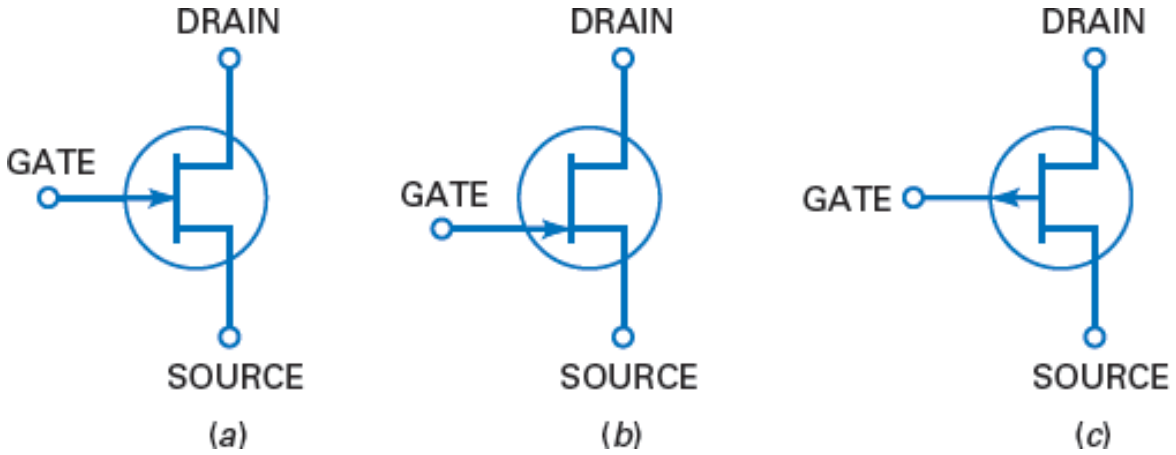


Figure-3 (a) Schematic symbol; (b) off set-gate symbol; (c) p-channel symbol

Example-1

A 2N5486 JFET has a gate current of 1 nA when the reverse gate voltage is 20 V. What is the input resistance of this JFET?

SOLUTION

Use Ohm's law to calculate:

$$R_{in} = \frac{20\ V}{1\ nA} = 20,000\ M\Omega$$

PRACTICE PROBLEM 11-1

In Example-1, calculate the input resistance if the JFET's gate current is 2 nA.

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1.3 Difference between BJT and FET

Bipolar Junction Transistor (BJT)	Field Effect Transistor (FET)
Bipolar device. In BJT, the operation is depends upon both minority and majority current carriers. Thus it is known as Bipolar device.	Unipolar device. In FET, the operation is depends upon the flow of majority carriers only i.e. holes for P-Channel FET and electrons for N-Channel FET. Therefore they are called as Unipolar devices.
Lower switching speed. BJT suffers from minority carrier storage effects. So it has lower switching speed and cut off frequencies.	Higher switching speed FET does not suffers from minority carrier storage effects. So it has higher switching speed and cut off frequencies.
Current controlled device. In BJT, the base current controls the output current.	Voltage controlled device. In FET, the Gate voltage controls the output current.
Less input impedance. The input circuit of BJT is forward biased. So BJT has low input impedance.	High input impedance The input circuit of FET is reverse biased. So FET exhibits much higher input impedance (>100Mohms) and lower output impedance. As they have high degree of isolation between input and output, FET acts as a buffer amplifier.
Comparatively BJT has more noisy operation.	Less noisy FET don't have junctions and the current conduction is happening through N-type or P-type semiconductor material. So its operation is less noisy.
Relatively more affected by radiations Due to reduction in minority carrier lifetime, the performance of BJT is degraded by neutron radiation.	Less affected. As FET operation does not depends upon the minority carriers, they can tolerate much higher level of radiation.
Lesser thermal stability. BJT has a positive temperature coefficient at high current levels. It leads to thermal breakdown.	More thermal stability. FET has a negative temperature coefficient at high current levels. It prevents the FET from thermal breakdown issue.
In IC fabrication, BJTs are occupying more space.	FETs are easier to fabricate and occupying less space.
BJTs are cheaper to produce.	Comparatively FETs are more costly.

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1.4 Drain Curves

- Figure-4a shows a JFET with normal biasing voltages. In this circuit, the gate-source voltage V_{GS} equals the gate supply voltage V_{GG}, and the drain-source voltage V_{DS} equals the drain supply voltage V_{DD}.

1.4.1 Maximum Drain Current

- If we short the gate to the source, as shown in Figure-4b, we will get maximum drain current because $V_{GS} = 0$. Figure-4c shows the graph of drain current I_D versus drain-source voltage V_{DS} for this shorted-gate condition.
- Notice how the drain current increases rapidly and then becomes almost horizontal when V_{DS} is greater than V_P.

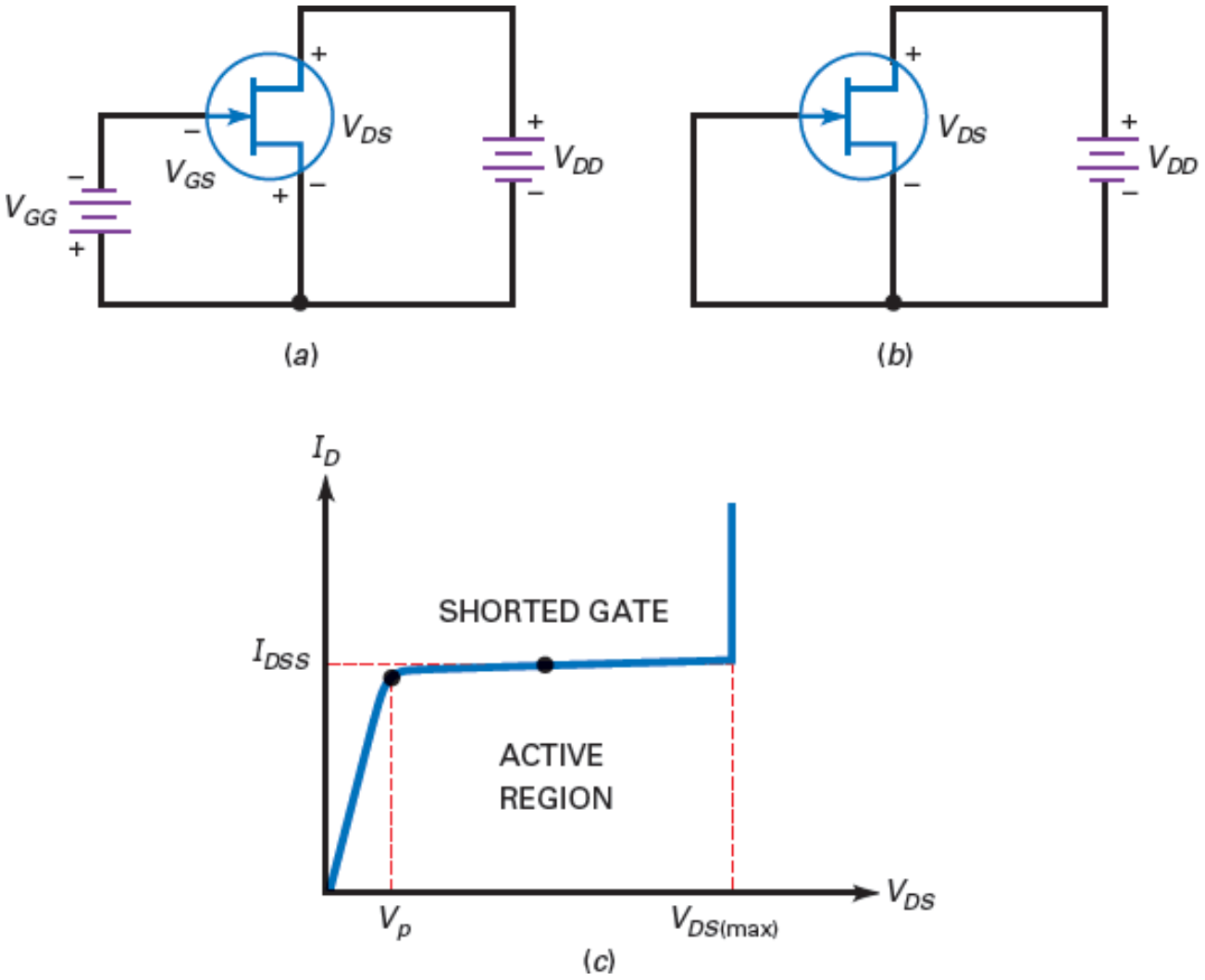


Figure-4 (a) Normal bias; (b) zero gate voltage; (c) shorted gate drain current

- Why does the drain current become almost constant? When V_{DS} increases, the depletion layers expand. When $V_{DS} = V_P$, the depletion layers are almost touching. The narrow conducting channel therefore pinches off or prevents a further increase in current.

- This is why the current has an upper limit of I_{DSS}. The active region of a JFET is between V_P and $V_{DS(max)}$. The minimum voltage V_P is called the pinch-off voltage, and the maximum voltage $V_{DS(max)}$ is the breakdown voltage. Between pinch-off and breakdown, the JFET acts like a current source of approximately I_{DSS} when V_{GS} = 0.
- I_{DSS} stands for the current drain to source with a shorted gate. This is the maximum drain current a JFET can produce. The data sheet of any JFET lists the value of I_{DSS}.
- This is one of the most important JFET quantities, and you should always look for it first because it is the upper limit on the JFET current.

1.4.2 The Ohmic Region

- In Figure-5, the pinch-off voltage separates two major operating regions of the JFET. The almost-horizontal region is the active region. The almost-vertical part of the drain curve below pinch-off is called the ohmic region.

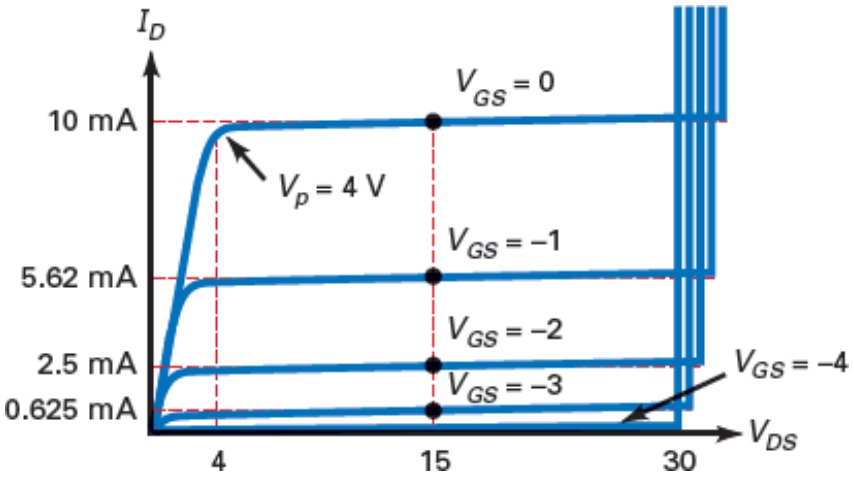


Figure-5 Drain Curves

- When operated in the ohmic region, a JFET is equivalent to a resistor with a value of approximately:

$$R_{DS} = \frac{VP}{I_{DSS}} \text{ ---------- (1)}$$

- R_{DS} is called the ohmic resistance of the JFET. In Figure-5, V_P = 4 V and I_{DSS} = 10 mA. Therefore, the ohmic resistance is:

$$R_{DS} = \frac{4\ V}{10\ mA} = 400\Omega$$

- If the JFET is operating anywhere in the ohmic region, it has an ohmic resistance of 400 Ω.

1.4.3 Gate Cutoff Voltage

- Figure-5 shows the drain curves for a JFET with an I_{DSS} of 10 mA.
- The top curve is always for V_{GS} = 0, the shorted-gate condition. In this example, the pinch-off voltage is 4 V and the breakdown voltage is 30 V. The next curve down is for V_{GS} = -1 V, the next for V_{GS} = -2 V, and so on. As you can see, the more negative the gate-source voltage, the smaller the drain current.

- The bottom curve is important. Notice that a V_{GS} of -4 V reduces the drain current to almost zero. This voltage is called the gate-source cutoff voltage and is symbolized by $V_{GS\,(off)}$ on data sheets.
- At this cutoff voltage, the depletion layers touch. In effect, the conducting channel disappears. This is why the drain current is approximately zero.
- In Figure-5, notice that $V_{GS\,(off)}$ = -4 V and V_P = 4 V
- This is not a coincidence. The two voltages always have the same magnitude because they are the values where the depletion layers touch or almost touch. Data sheets may list either quantity, and you are expected to know that the other has the same magnitude. As an equation:

$$V_{GS\,(off)} = -V_P \text{---------- (2)}$$

1.5 The Transconductance Curve

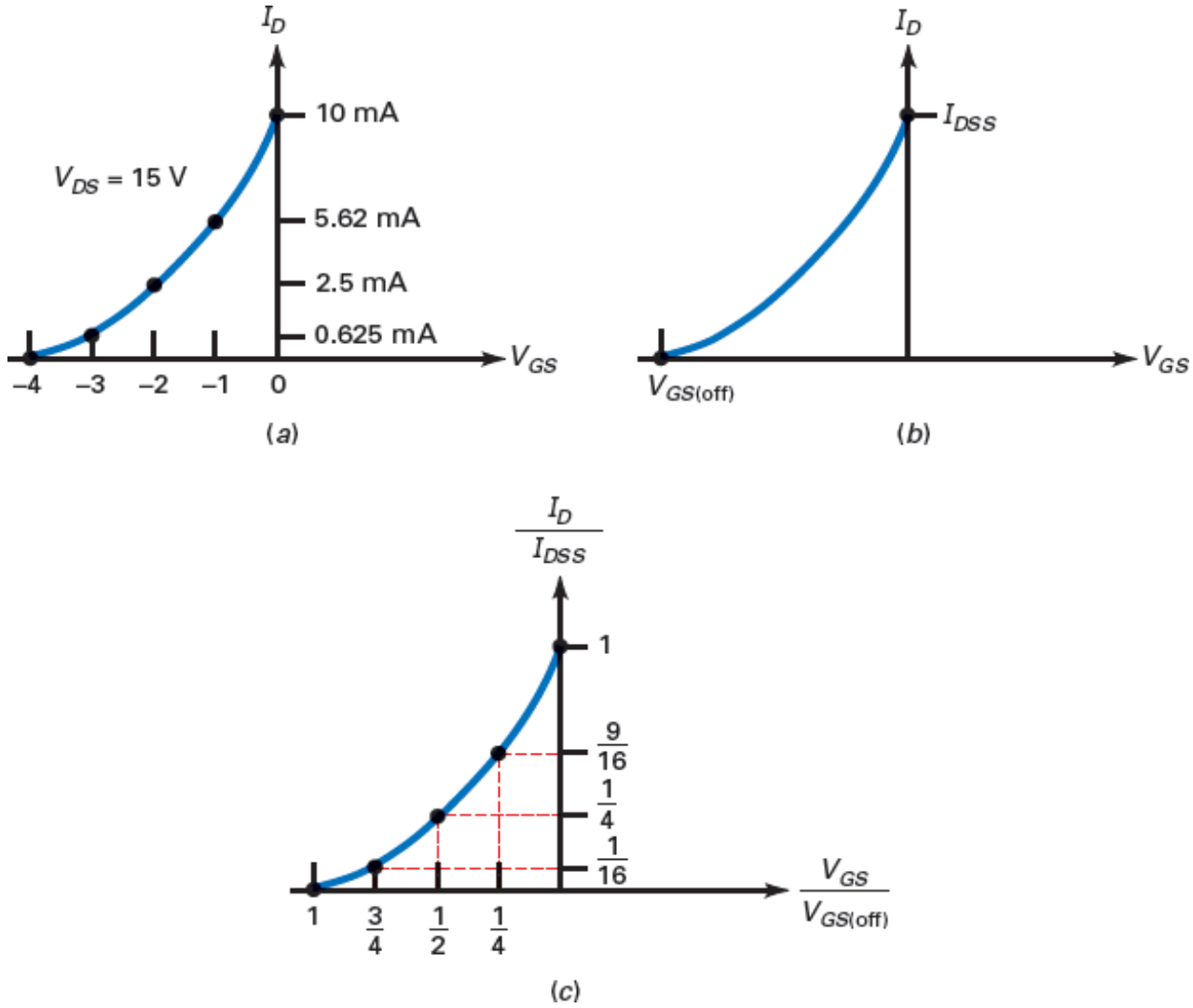


Figure-6 Transconductance curve

- The transconductance curve of a JFET is a graph of I_D versus V_{GS}. By reading the values of I_D and V_{GS} of each drain curve in Figure-5, we can plot the curve of Figure-6a. Notice that the curve is nonlinear because the current increases faster when V_{GS} approaches zero.

- Any JFET has a transconductance curve like Figure-6b. The end points on the curve are $V_{GS(off)}$ and I_{DSS}. The equation for this graph is:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \text{ ---------- (3)}$$

- Because of the squared quantity in this equation, JFETs are often called square-law devices. The squaring of the quantity produces the nonlinear curve of Figure-6b.
- Figure-6c shows a normalized transconductance curve. Normalized means that we are graphing ratios like I_D/I_{DSS} and $V_{GS}/V_{GS(off)}$.
- In Figure-6c, the half-cutoff point

$$\frac{V_{GS}}{V_{GS(off)}} = \frac{1}{2}$$

Produces a normalized current of:

$$\frac{I_{DS}}{I_{DSS}} = \frac{1}{4}$$

- In words: When the gate voltage is half the cutoff voltage, the drain current is one quarter of maximum.

1.6 Biasing in the Ohmic Region

- The JFET can be biased in the ohmic or in the active region. When biased in the ohmic region, the JFET is equivalent to a resistance. When biased in the active region, the JFET is equivalent to a current source. In this section, we discuss gate bias, the method used to bias a JFET in the ohmic region.

1.6.1 Gate Bias

- Figure-7a shows gate bias. A negative gate voltage of $-V_{GG}$ is applied to the gate through biasing resistor R_G. This sets up a drain current that is less than I_{DSS}.
- When the drain current flows through R_D, it sets up a drain voltage of:

$$V_D = V_{DD} - I_D R_D \text{ ---------- (4)}$$

- Gate bias is the worst way to bias a JFET in the active region because the Q point is too unstable.
- For example, a 2N5459 has the following spreads between minimum and maximum: I_{DSS} varies from 4 to 16 mA, and $V_{GS(off)}$ varies from -2 to -8 V.
- Figure-7b shows the minimum and maximum transconductance curves. If a gate bias of -1 V is used with this JFET, we get the minimum and maximum Q points shown. Q_1 has a drain current of 12.3 mA, and Q_2 has a drain current of only 1 mA.

1.6.2 Hard Saturation

- Although not suitable for active-region biasing, gate bias is perfect for ohmic region biasing because stability of the Q point does not matter. Figure-7c shows how to bias a JFET in the ohmic region. The upper end of the dc load line has a drain saturation current of:

$$I_{D(sat)} = \frac{V_{DD}}{R_D}$$

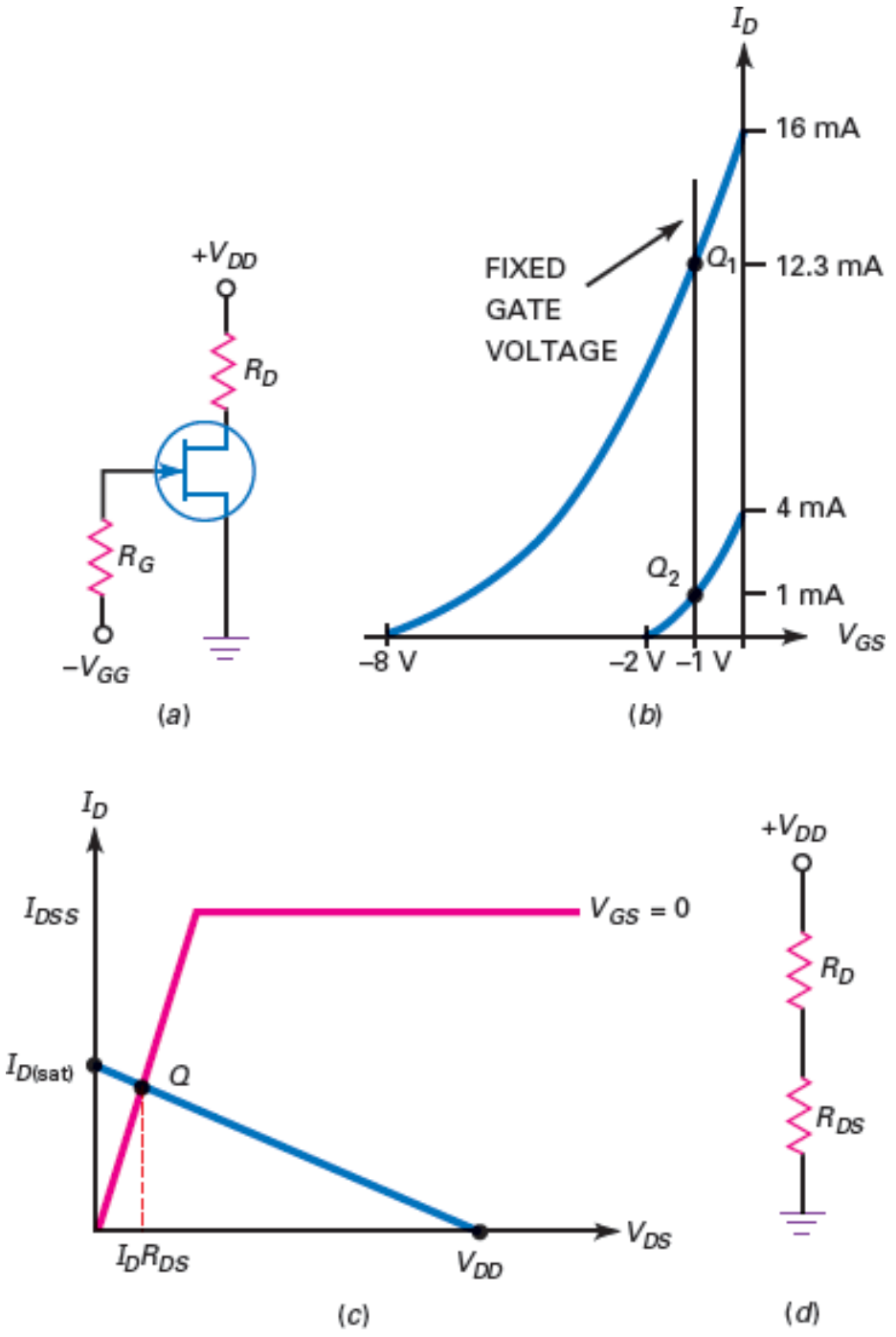


Figure-7 (a) Gate bias; (b) Q point unstable in active region; (c) biased in ohmic region; (d) JFET is equivalent to resistance

- To ensure that a JFET is biased in the ohmic region, all we need to do is use $V_{GS} = 0$ and:

$$I_{D(sat)} \ll I_{DSS} \text{---------- (5)}$$

- The symbol << means "much less than." This equation says that the drain saturation current must be much less than the maximum drain current. For instance, if a JFET has $I_{DSS} = 10$ mA, hard saturation will occur if $V_{GS} = 0$ and $I_{D(sat)} = 1$ mA.

- When a JFET is biased in the ohmic region, we can replace it by a resistance of R_{DS}, as shown in Figure-7d. With this equivalent circuit, we can calculate the drain voltage. When R_{DS} is much smaller than R_D, the drain voltage is close to zero.

1.7 Biasing in the Active Region

- JFET amplifiers need to have a Q point in the active region. Because of the large spread in JFET parameters, we cannot use gate bias. Instead, we need to use other biasing methods. Some of these methods are similar to those used with bipolar junction transistors.
- The choice of analysis technique depends on the level of accuracy needed. For example, when doing preliminary analysis and troubleshooting of biasing circuits, it is often desirable to use ideal values and circuit approximations.
- In JFET circuits, this means that we will often ignore V_{GS} values. Usually, the ideal answers will have an error of less that 10 percent. When closer analysis is called for, we can use graphical solutions to determine a circuit's Q point.
- If you are designing JFET circuits or need even greater accuracy, you should use a circuit simulator like Multisim.

1.7.1 Self-Bias

- Figure-8a shows self-bias. Since drain current flows through the source resistor R_S, a voltage exists between the source and ground, given by:

$$V_S = I_D R_S \text{ ---------- (6)}$$

- Since V_G is zero:

$$V_{GS} = -I_D R_S \text{ ---------- (7)}$$

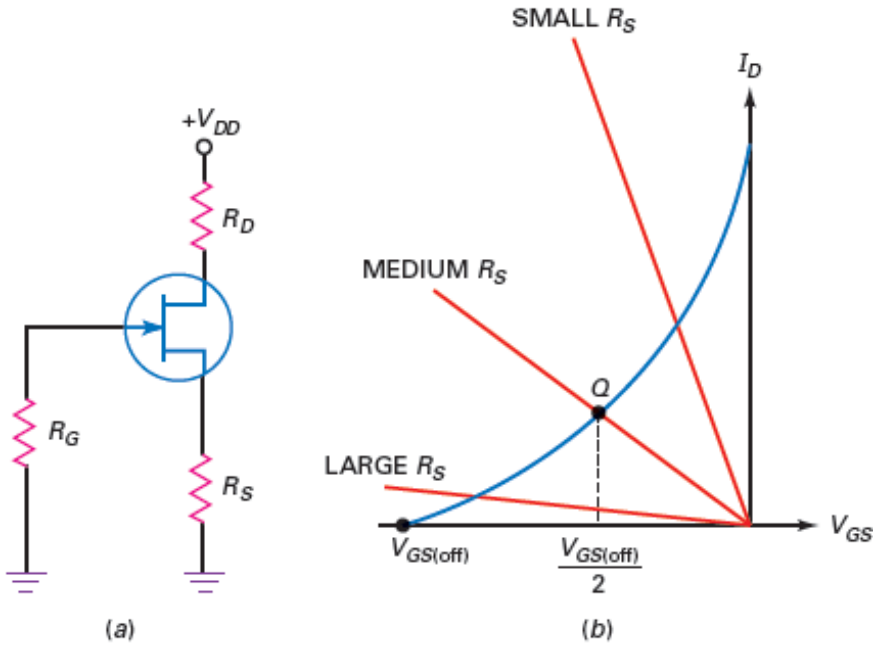


Figure-8 Self Bias

- This says that the gate-source voltage equals the negative of the voltage across the source resistor.

- Basically, the circuit creates its own bias by using the voltage developed a cross R_S to reverse-bias the gate. Figure-8b shows the effect of different source resistors. There is a medium value of R_S at which the gate-source voltage is half of the cutoff voltage. An approximation for this medium resistance is:

$$R_S \approx R_{DS} \text{---------- (8)}$$

- This equation says that the source resistance should equal the ohmic resistance of the JFET. When this condition is satisfied, the V_{GS} is roughly half the cutoff voltage and the drain current is roughly one-quarter of I_{DSS}.
- When a JFET's transconductance curves are known, we can analyze a self-bias circuit using graphical methods. Suppose a self-bias JFET has the transconductance curve shown in Figure-9.

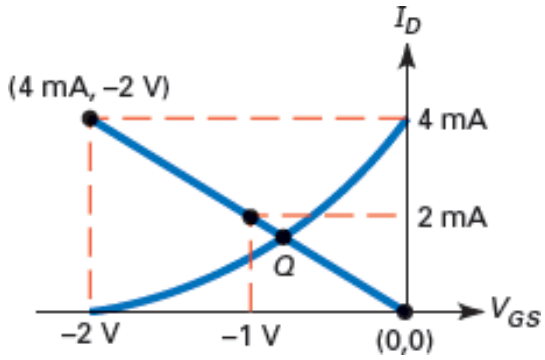


Figure-9 Self bias Q point

- The maximum drain current is 4 mA, and the gate voltage has to be between 0 and -2 V. By graphing Eq. (7), we can find out where it intersects the transconductance curve and determine the values of V_{GS} and I_D. Since Eq. (7) is a linear equation, all we have to do is plot two points and draw a line through them.
- Suppose the source resistance is 500 Ω. Then Eq. (7) becomes:

$$V_{GS} = -ID\ (500\ \Omega)$$

- Since any two points can be used, we choose the two convenient points corresponding to

$$I_D = -(0)(500\ \Omega) = 0$$

Therefore, the coordinates for the first point are (0, 0), which is the origin. To get the second point, find V_{GS} for $I_D = I_{DSS}$. In this case, I_D = 4 mA and V_{GS} = - (4 mA) (500 Ω) = -2 V; therefore, the coordinates of the second point are at (4 mA, -2 V).

- We now have two points on the graph of Eq. (7). The two points are (0, 0) and (4 mA, -2 V). By plotting these two points as shown in Figure-9, we can draw a straight line through the two points as shown.
- This line will, of course, intersect the transconductance curve. This intersection point is the operating point of the self-biased JFET. As you can see, the drain current is slightly less than 2 mA, and the gate-source voltage is slightly less than -1 V.
- In summary, here is a process for finding the Q point of any self-biased JFET, provided you have the transconductance curve. If the curve is not available, you can use the and I_{DSS} rated values, along with the square law equation (3), to develop one:
  1. Multiply I_{DSS} by R_S to get V_{GS} for the second point.
  2. Plot the second point (I_{DSS}, V_{GS}).

3. Draw a line through the origin and the second point.
4. Read the coordinates of the intersection point.

- The Q point with self-bias is not extremely stable. Because of this, self-bias is used only with small-signal amplifiers. This is why you may see self- biased JFET circuits near the front end of communication receivers where the signal is small.

1.7.2 Voltage-Divider Bias

- Figure-10a shows voltage-divider bias. The voltage divider produces a gate voltage that is a fraction of the supply voltage.

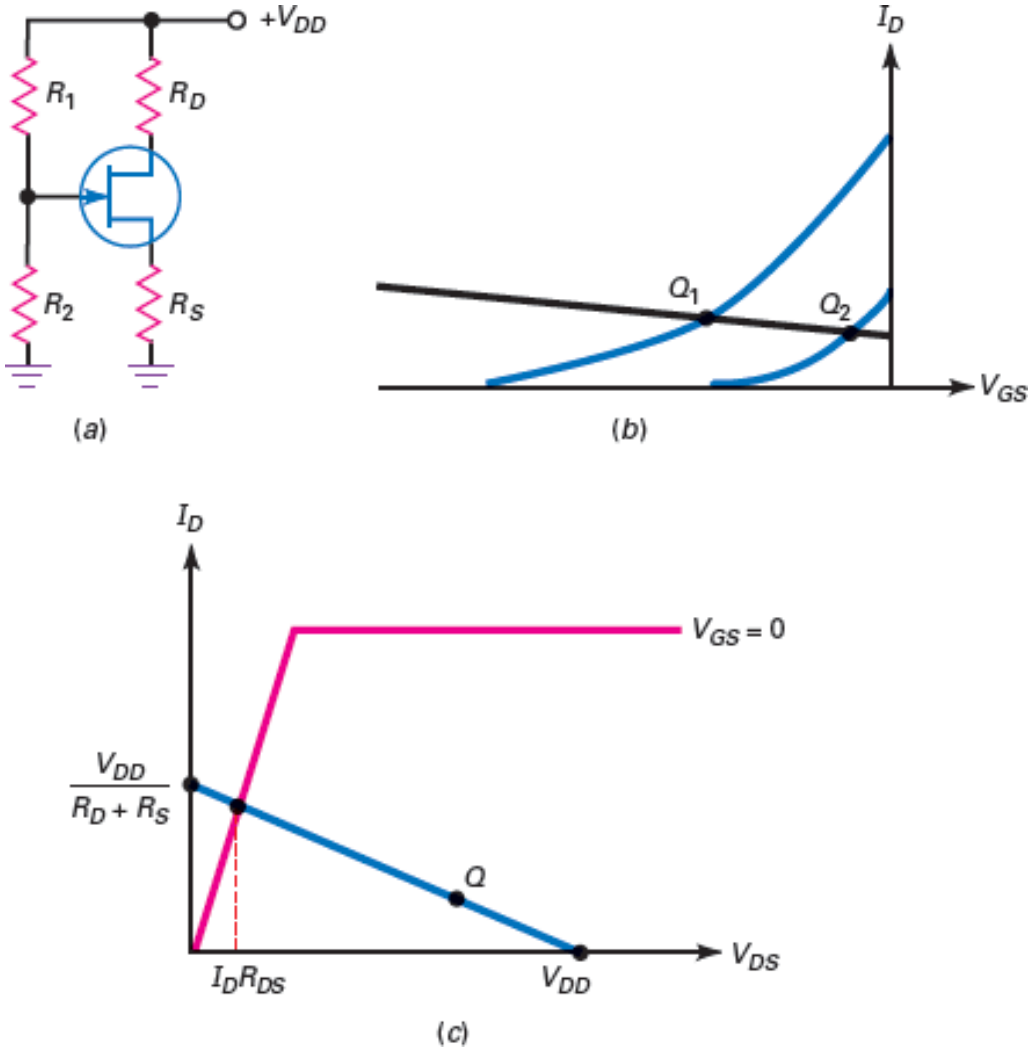


Figure-10 Voltage-divider bias

- By subtracting the gate-source voltage, we get the voltage across the source resistor:

$$V_S = V_G - V_{GS} \text{ ---------- (9)}$$

- Since V_{GS} is a negative, the source voltage will be slightly larger than the gate voltage. When you divide this source voltage by the source resistance, you get the drain current:

$$I_D = \frac{VG - VGS}{R_S} \approx \frac{VG}{R_S} \text{ ---------- (10)}$$

- When the gate voltage is large, it can swamp out the variations in V_{GS} from one JFET to the next. Ideally, the drain current equals the gate voltage divided by the source resistance. As a result, the drain current is almost constant for any JFET, as shown in Figure-10b.
- Figure-10c shows the dc load line. For an amplifier, the Q point has to be in the active region. This means that V_{DS} must be greater than $I_D R_{DS}$ (ohmic region) and less than V_{DD} (cutoff).
- When a large supply voltage is available, voltage-divider bias can set up a stable Q point. When more accuracy is needed in determining the Q point for a voltage divider bias circuit, a graphical method can be used.
- This is especially true when the minimum and maximum V_{GS} values for a JFET vary several volts from each other. In Figure-10a, the voltage applied to the gate is:

$$V_G = \frac{R2}{R_1 + R_2}(V_{DD}) \text{---------- (11)}$$

- Using transconductance curves, as in Figure-11, plot the V_G value on the horizontal, or x-axis, of the graph. This becomes one point on our bias line.

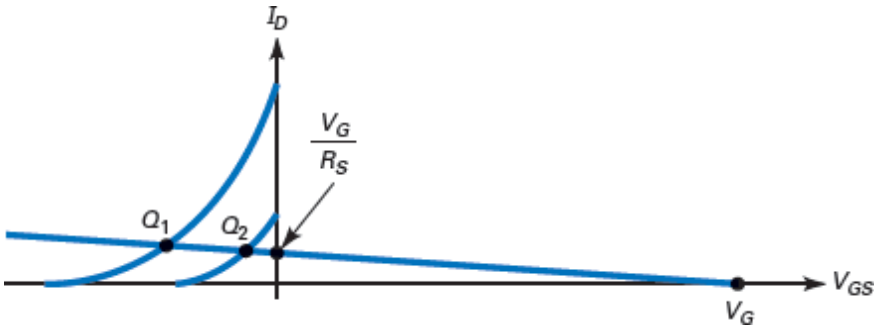


Figure-11 VDB Q point

- To get the second point, use Eq. (10) with V_{GS} = 0 V to determine I_D. This second point, where $I_D = V_G/R_S$, is plotted on the vertical, or y-axis, of the transconductance curve.
- Next, draw a line between these two points and extend the line so it intersects the transconductance curves. Finally, read the coordinates of the intersection points.

1.7.3 Two-Supply Source Bias

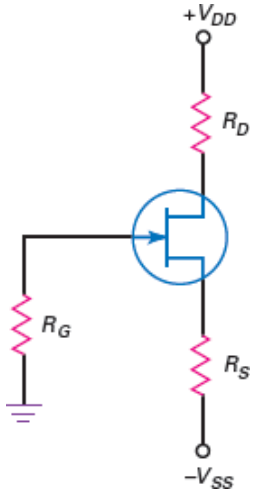


Figure-12 Two-supply source bias

- Figure-12 shows two-supply source bias. The drain current is given by:

$$I_D = \frac{VSS - VGS}{R_S} \approx \frac{VSS}{R_S} \text{ ---------- (12)}$$

- Again, the idea is to swamp out the variations in V_{GS} by making V_{SS} much larger than V_{GS}. Ideally, the drain current equals the source supply voltage divided by the source resistance.
- In this case, the drain current is almost constant in spite of JFET replacement and temperature change.

1.7.4 Current-Source Bias

- When the drain supply voltage is not large, there may not be enough gate voltage to swamp out the variations in V_{GS}. In this case, a designer may prefer to use the current-source bias of Figure-13a. In this circuit, the bipolar junction transistor pumps a fixed current through the JFET. The drain current is given by:

$$I_D = \frac{VEE - VBE}{R_E} \text{ ---------- (13)}$$

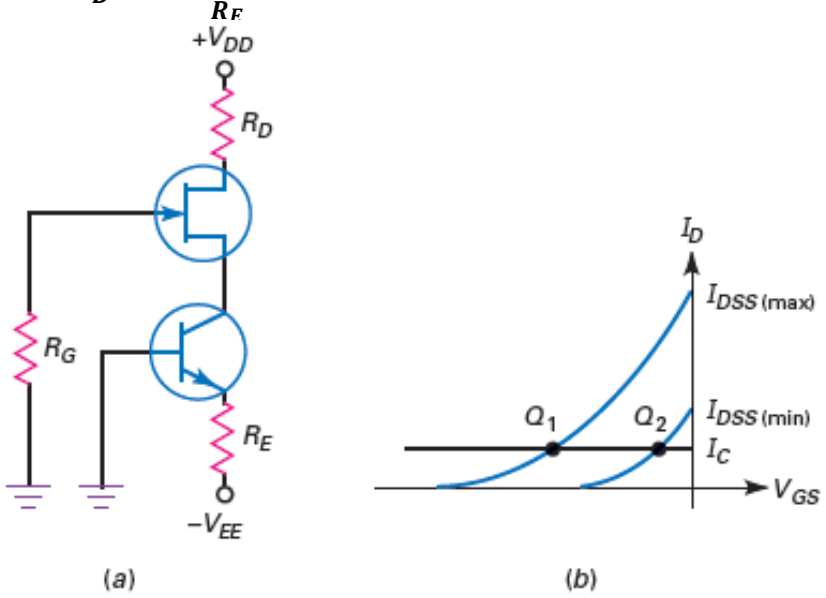


Figure-13 Current-source bias

- Figure-13b illustrates how effective current-source bias is. Both Q points have the same current. Although V_{GS} is different for each Q point, V_{GS} no longer has an effect on the value of drain current.

1.8 Transconductance

- To analyze JFET amplifiers, we need to discuss transconductance, designated ***gm*** and defined as:

$$g_m = \frac{id}{v_{gs}} \text{ ---------- (14)}$$

- This says that transconductance equals the ac drain current divided by the ac gate-source voltage. Transconductance tells us how effective the gate-source voltage is in controlling the drain current. The higher the transconductance, the more control the gate voltage has over the drain current.

- For instance, if i_d = 0.2 $mA_{p\text{-}p}$ when v_{gs} = 0.1 $V_{p\text{-}p}$, then:

$$g_m = \frac{0.2\ mA}{0.1\ V} = 2(10^{-3})\text{℧} = 2000\mu\text{℧}$$

- On the other hand, if i_d = 1 $mA_{p\text{-}p}$ when v_{gs} = 0.1 $V_{p\text{-}p}$, then:

$$g_m = \frac{1\ mA}{0.1\ V} = 10,000\mu\text{℧}$$

- In the second case, the higher transconductance means that the gate is more effective in controlling the drain current.

1.8.1 Siemen

- The unit mho is the ratio of current to voltage. An equivalent and modern unit for the mho is the Siemen(S), so the foregoing answers can be written as 2000 µS and 10,000 µS. On data sheets, either quantity (mho or Siemen) may be used. Data sheets may also use the symbol g_{fs} instead of g_m.
- As an example, the data sheet of a 2N5451 lists a g_{fs} of 2000 µS for a drain current of 1 mA. This is identical to saying that the 2N5451 has a g_m of 2000 µmho for a drain current of 1 mA.

1.8.2 Slope of Transconductance Curve

- Figure-14a brings out the meaning of g_m in terms of the transconductance curve. Between points A and B, a change in V_{GS} produces a change in I_D. The change in I_D divided by the change in V_{GS} is the value of g_m between A and B.
- If we select another pair of points farther up the curve at C and D, we get a bigger change in ID for the same change in V_{GS}. Therefore, gm has a larger value higher up the curve. Stated another way, gm is the slope of the transconductance curve. The steeper the curve is at the Q point, the higher the transconductance.

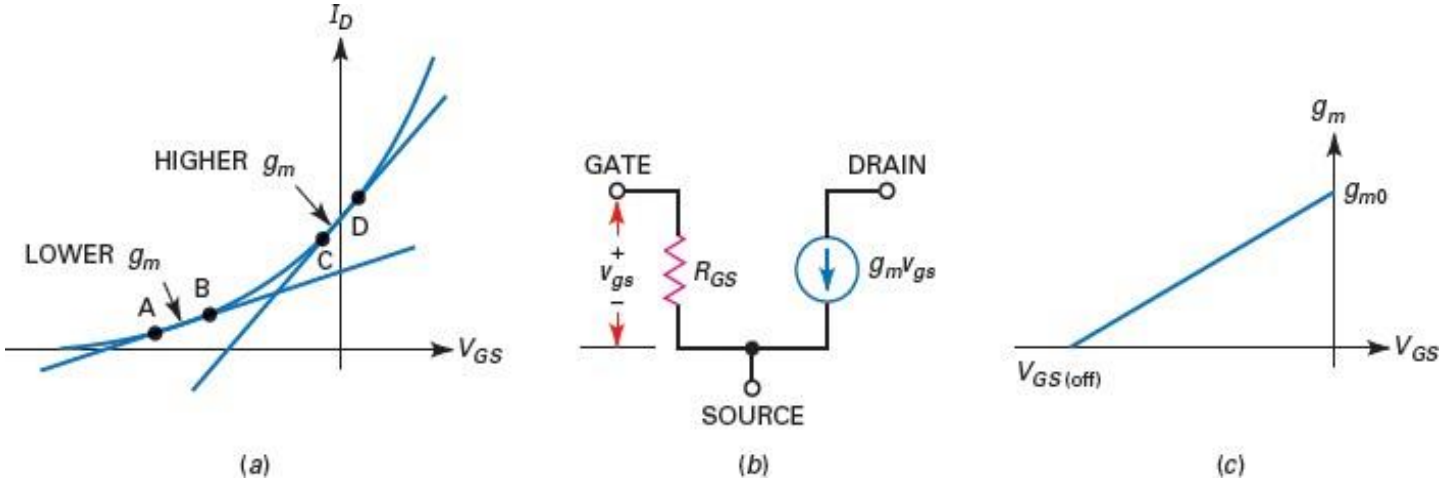


Figure-14 (a) Transconductance; (b) ac-equivalent circuit; (c) variation of g_m

- Figure-14b shows an ac-equivalent circuit for a JFET. A very high resistance R_{GS} is between the gate and the source. The drain of a JFET acts like a current source with a value of $g_m v_{gs}$. Given the values of g_m and v_{gs}, we can calculate the ac drain current.

1.8.3 Transconductance and Gate-Source Cutoff Voltage

- The quantity $V_{GS(off)}$ is difficult to measure accurately. On the other hand, I_{DSS} and g_{m0} are easy to measure with high accuracy. For this reason, $V_{GS(off)}$ is often calculated with the following equation:

$$V_{GS(off)} = \frac{-2IDSS}{g_{m0}} \text{ ---------- (15)}$$

- In this equation, g_{m0} is the value of transconductance when $V_{GS} = 0$. Typically, a manufacturer will use the foregoing equation to calculate the value of $V_{GS(off)}$ for use on data sheets.
- The quantity g_{m0} is the maximum value of g_m for a JFET because it occurs when $V_{GS} = 0$. When V_{GS} becomes negative, g_m decreases. Here is the equation for calculating g_m for any value of V_{GS}:

$$g_m = g_{m0}\ \left(1 - \frac{VGS}{V_{GS(off)}}\right) \text{ ---------- (16)}$$

- Notice that g_m decreases linearly when V_{GS} becomes more negative, as shown in Figure-14c. Changing the value of g_m is useful in automatic gain control, which is discussed later.

1.9 JFET Amplifiers

- Figure-15a shows a common-source (CS) amplifier. The coupling and bypass capacitors are ac shorts. Because of this, the signal is coupled directly into the gate. Since the source is bypassed to ground, all of the ac input voltage appears between the gate and the source.

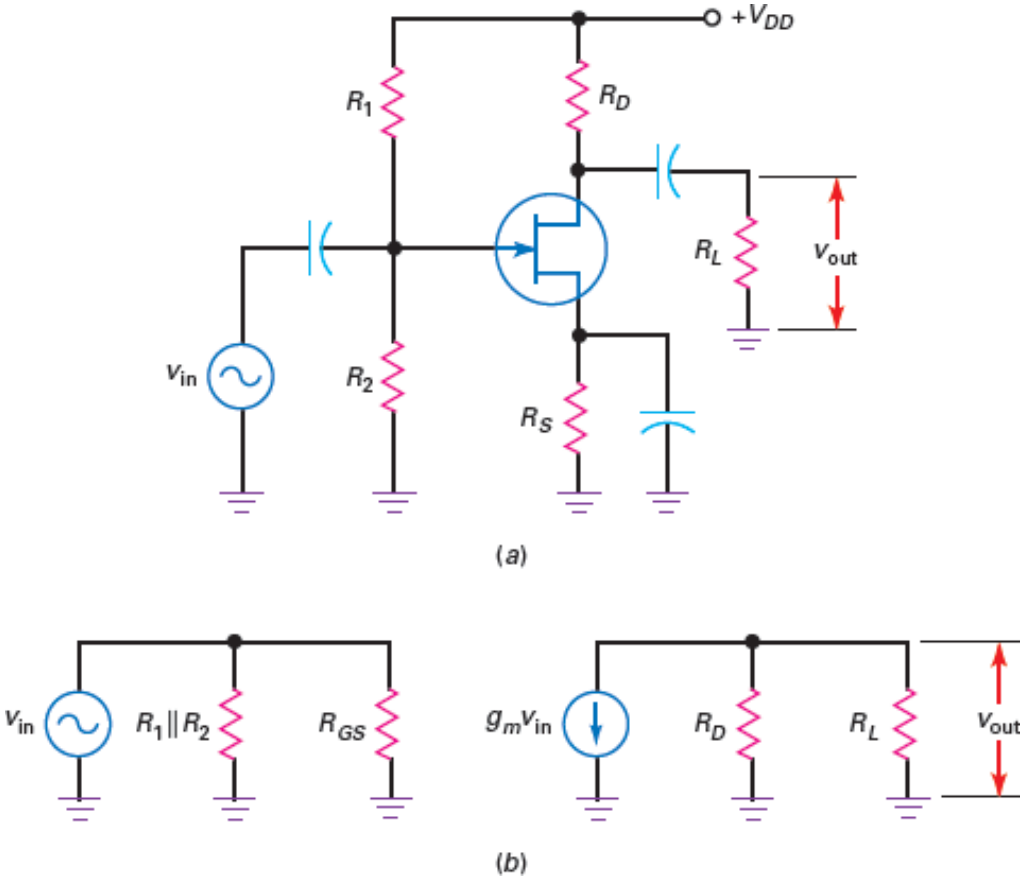


Figure-15 (a) CS amplifier; (b) ac-equivalent circuit

- This produces an ac drain current. Since the ac drain current flows through the drain resistor, we get an amplified and inverted ac output voltage. This output signal is then coupled to the load resistor.

1.9.1 Voltage Gain of CS Amplifier

- Figure-15b shows the ac-equivalent circuit. The ac drain resistance r_d is defined as:

$$r_d = R_D \| R_L$$

- The voltage gain is:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_m V_{in} r_d}{V_{in}}$$

- which simplifies to:

$$A_v = g_m r_d \text{ ---------- (17)}$$

- This says that the voltage gain of a CS amplifier equals the transconductance times the ac drain resistance.

1.9.2 Input and Output Impedance of CS Amplifier

- Since a JFET normally has a reverse biased gate-source junction, its input resistance at the gate R_{GS} is very large. R_{GS} can be approximated by using values taken
- from the JFET's data sheet and can be found by:

$$R_{GS} = \frac{VGS}{I_{GSS}} \text{ ---------- (18)}$$

- As an example, if I_{GSS} is -2.0 nA when V_{GS} is -15 V, R_{GS} would equal 7500 MΩ. As shown in Figure-15b, the input impedance of the stage is:

$$Z_{in\,(stage)} = R_1 \| R_2 \| R_{GS}$$

- Because R_{GS} is normally very large, as compared to the input biasing resistors, the input impedance of the stage can be reduced to:

$$Z_{in\,(stage)} = R_1 \| R_2 \text{ ---------- (19)}$$

- In a CS amplifier, $Z_{out(stage)}$ looks back into the circuit from the load resistor R_L. In Figure-15b, the load resistance sees R_D in parallel with a constant current source, which ideally is an open. Therefore:

$$Z_{out\,(stage)} = R_D \text{ ---------- (20)}$$

1.9.3 Source Follower

- Figure-16a shows a common-drain (CD) amplifier, also known as a source follower. The input signal drives the gate, and the output signal is coupled from the source to the load resistor. Like the emitter follower, the source follower has a voltage gain less than 1.
- The main advantage of the source follower is its very high input resistance and its low output resistance. Often, you will see a source follower used at the front end of a system, followed by bipolar stages of voltage gain.
- In Figure-16b, the ac source resistance is defined as:

$$r_s = R_S \| R_L$$

- The voltage gain of a source follower is found by:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{i_d r_S}{v_{gs} + i_d r_S} = \frac{v_{gs} g_m r_S}{v_{gs} + v_{gs} g_m r_S}$$

Where $i_d = g_m v_{gs}$

Which reduces to:

$$A_v = \frac{gmrS}{1+g_m r_S} \text{ ---------- (21)}$$

- Because the denominator is always greater than the numerator, the voltage gain is always less than 1.

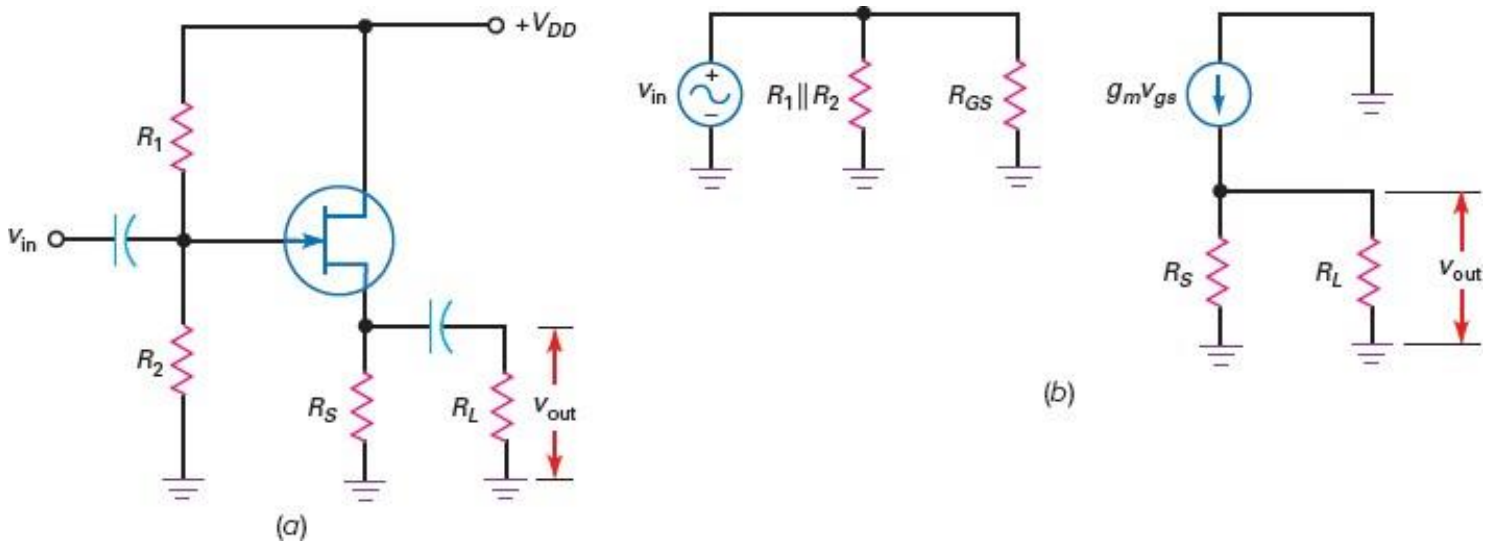


Figure-16 (a) Source follower (b) ac-equivalent

- Figure-16b shows that the input impedance of the source follower is the same as the CS amplifier:

$$Z_{in\,(stage)} = R_1 \| R_2 \| R_{GS}$$

- Which simplifies to:

$$Z_{in\,(stage)} = R_1 \| R_2$$

- The output impedance $Z_{out(stage)}$ is found by looking back into the circuit from the load:

$$Z_{out\,(stage)} = R_s \| R_{in\,(source)}$$

- The resistance looking into the JFET's source is:

$$R_{in\,(source)} = \frac{V_{source}}{I_{source}} = \frac{v_{gs}}{i_s}$$

Since, $v_{gs} = \frac{i_d}{g_m}$ and $i_d = i_s$ and $R_{in\,(source)} = \frac{\frac{i_d}{g_m}}{i_d} = \frac{1}{g_m}$

- Therefore, the output impedance of the source follower is:

$$Z_{out\,(stage)} = R_s \| \frac{1}{g_m} \text{ ---------- (22)}$$

Unit 5: Field effect transistors (FET) and its Biasing

1.10 The JFET Analog Switch

- Besides the source follower, another major application of the JFET is analog switching. In this application, the JFET acts as a switch that either transmits or blocks a small ac signal. To get this type of action, the gate-source voltage V_{GS} has only two values: either zero or a value that is greater than $V_{GS(off)}$. In this way, the JFET operates either in the ohmic region or in the cutoff region.

1.10.1 Shunt Switch

- Figure-17a shows a JFET shunt switch. The JFET is either conducting or cut off, depending on whether V_{GS} is high or low. When V_{GS} is high (0 V), the JFET operates in the ohmic region. When V_{GS} is low, the JFET is cut off. Because of this, we can use Figure-17b as an equivalent circuit.

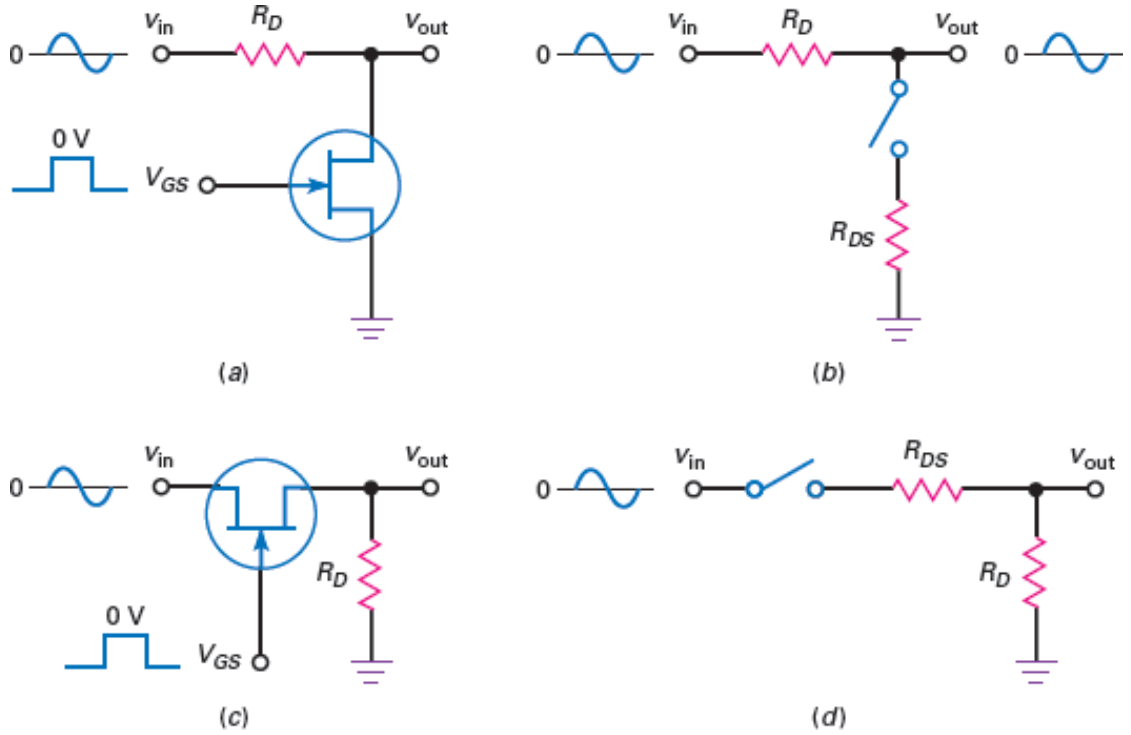


Figure-17 JFET analog switches: (a) Shunt type; (b) shunt-equivalent circuit; (c) series type; (d) series-equivalent circuit

- For normal operation, the ac input voltage must be a small signal, typically less than 100 mV. A small signal ensures that the JFET remains in the ohmic region when the ac signal reaches its positive peak. Also, RD is much greater than R_{DS} to ensure hard saturation: $R_D >> R_{DS}$
- When V_{GS} is high, the JFET operates in the ohmic region and the switch of Figure-17b is closed. Since R_{DS} is much smaller than R_D, V_{out} is much smaller than V_{in}. When V_{GS} is low, the JFET cuts off and the switch of Figure-17b opens. In this case, $V_{out} = V_{in}$. Therefore, the JFET shunt switch either transmits the ac signal or blocks it.

1.10.2 Series Switch

- Figure-17c shows a JFET series switch, and Figure-17d is its equivalent circuit. When V_{GS} is high, the switch is closed and the JFET is equivalent to a resistance of R_{DS}.

- In this case, the output approximately equals the input. When V_{GS} is low, the JFET is open and V_{out} is approximately zero. The on-off ratio of a switch is defined as the maximum output voltage divided by the minimum output voltage:

$$On - Off\ Ratio = \frac{v_{out\ (max)}}{v_{out\ (min)}} \text{ ---------- (23)}$$

- When a high on-off ratio is important, the JFET series switch is a better choice because its on-off ratio is higher than that of the JFET shunt switch.

1.10.3 Chopper

- Figure-18 shows a JFET chopper. The gate voltage is a continuous square wave that continuously switches the JFET on and off. The input voltage is a rectangular pulse with a value of V_{DC}. Because of the square wave on the gate, the output is chopped (switched on and off), as shown.

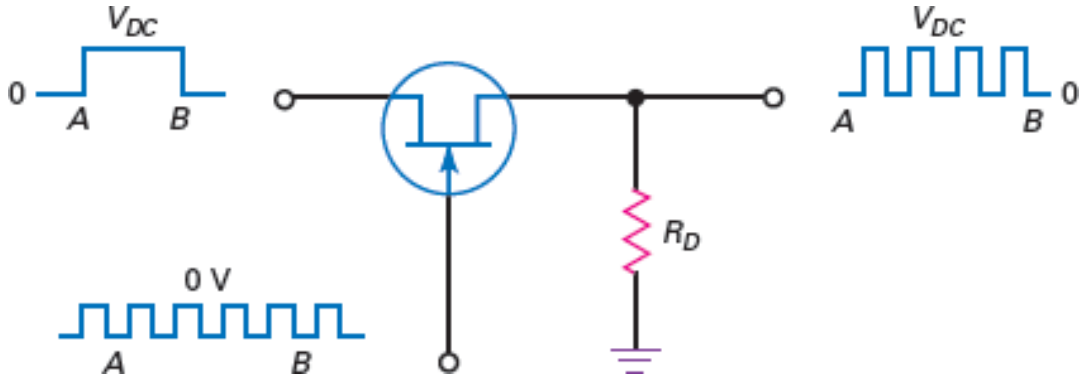


Figure-18 Chopper

- A JFET chopper can use either a shunt or a series switch. Basically, the circuit converts a dc input voltage to a square-wave output. The peak value of the chopped output is V_{DC}. As will be described later, a JFET chopper can be used to build a dc amplifier, a circuit that can amplify frequencies all the way down to zero frequencies.

1.11 Other JFET Applications

- A JFET cannot compete with a bipolar transistor for most amplifier applications. But its unusual properties make it a better choice in special applications. In this section, we discuss those applications where a JFET has a clear-cut advantage over the bipolar transistor.

1.11.1 Multiplexing

- Multiplex means "many into one." Figure-19 shows an analog multiplexer, a circuit that steers one or more of the input signals to the output line.
- Each JFET acts like a series switch. The control signals (V_1, V_2, and V_3) turn the JFETs on and off. When a control signal is high, its input signal is transmitted to the output.
- For instance, if V_1 is high and the others are low, the output is a sine wave. If V_2 is high and the others are low, the output is a triangular wave. When V_3 is the high input, the output is a square wave.
- Normally, only one of the control signals is high; this ensures that only one of the input signals is transmitted to the output.

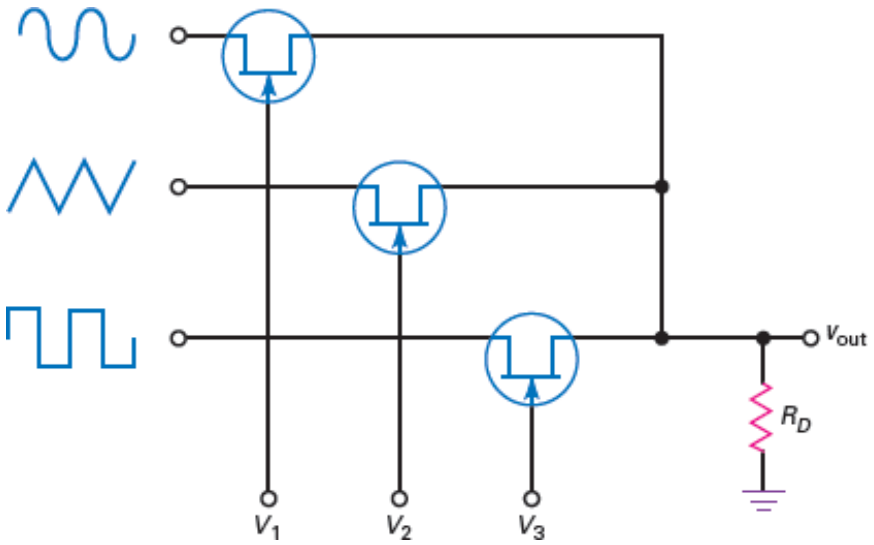
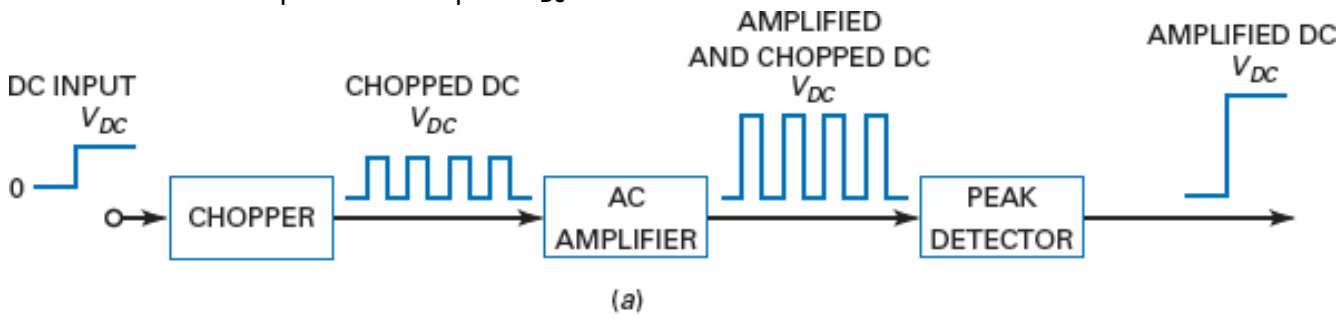


Figure-19 Multiplexer

1.11.2 Chopper Amplifiers

- We can build a direct-coupled amplifier by leaving out the coupling and bypass capacitors and connecting the output of each stage directly to the input of the next stage. In this way, dc voltages are coupled, as are ac voltages.
- Circuits that can amplify dc signals are called dc amplifiers. The major disadvantage of direct coupling is drift, a slow shift in the final dc output voltage produced by minor changes in supply voltage, transistor parameters, and temperature variations.
- Figure-20a shows one way to overcome the drift problem of direct coupling. Instead of using direct coupling, we use a JFET chopper to convert the input dc voltage to a square wave. The peak value of this square wave equals V_{DC}.



(*a*)

(*b*)

Figure-20 Chopper amplifier

- Because the square wave is an ac signal, we can use a conventional ac amplifier, one with coupling and bypass capacitors. The amplified output can then be peak detected to recover an amplified dc signal.
- A chopper amplifier can amplify low-frequency signals as well as dc signals. If the input is a low-frequency signal, it gets chopped into the ac waveform of Figure-20b. This chopped signal can be amplified by an ac amplifier.
- The amplified signal can then be peak-detected to recover the original input signal.

1.11.3 Buffer Amplifier

- Figure-21 shows a buffer amplifier, a stage that isolates the preceding stage from the following stage. Ideally, a buffer should have a high input impedance. If it does, almost all the Thevenin voltage from stage A appears at the buffer input.
- The buffer should also have a low output impedance. This ensures that all its output voltage reaches the input of stage B.

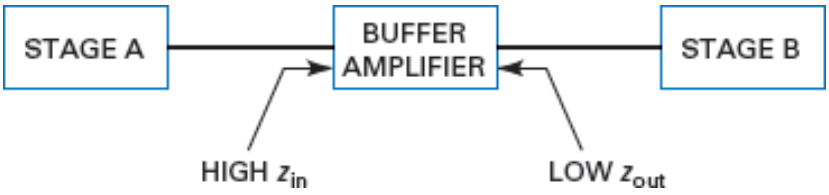


Figure-21 Buffer amplifiers isolates stages A and B

- The source follower is an excellent buffer amplifier because of its high input impedance (well into the mega-ohms at low frequencies) and its low output impedance (typically a few hundred ohms).
- The high input impedance means light loading of stage A. The low output impedance means that the buffer can drive heavy loads (small load resistances).

1.11.4 Low-Noise Amplifier

- Noise is any unwanted disturbance superimposed on a useful signal. Noise interferes with the information contained in the signal. For instance, the noise in television receivers produces small white or black spots on the picture.
- Severe noise can wipe out the picture altogether. Similarly, the noise in radio receivers produces crackling and hissing, which sometimes completely masks the signal.
- Noise is independent of the signal because it exists even when the signal is off. The JFET is an outstanding low-noise device because it produces much less noise than a bipolar junction transistor.
- Low noise is very important at the front end of receivers because the later stages amplify front-end noise along with the signal. If we use a JFET amplifier at the front end, we get less amplified noise at the final output.
- Other circuits near the front end of receivers include frequency mixers and oscillators. A frequency mixer is a circuit that converts a higher frequency to a lower one. An oscillator is a circuit that generates an ac signal.
- JFETs are often used for VHF/UHF amplifiers, mixers, and oscillators. VHF stands for “very high

- frequencies" (30 to 300 MHz), and UHF, for "ultra high frequencies") (300 to 3000 MHz).

1.11.5 Voltage-Controlled Resistance

- When a JFET operates in the ohmic region, it usually has V_{GS} = 0 to ensure hard saturation. But there is an exception. It is possible to operate a JFET in the ohmic region with V_{GS} values between 0 and $V_{GS(off)}$. In this case, the JFET can act like a voltage-controlled resistance.
- Figure-22 shows the drain curves of a 2N5951 near the origin with V_{DS} less than 100 mV. In this region, the small-signal resistance r_{ds} is defined as the drain voltage divided by the drain current:

$$r_{ds} = \frac{VDS}{I_D} \text{ ---------- (24)}$$

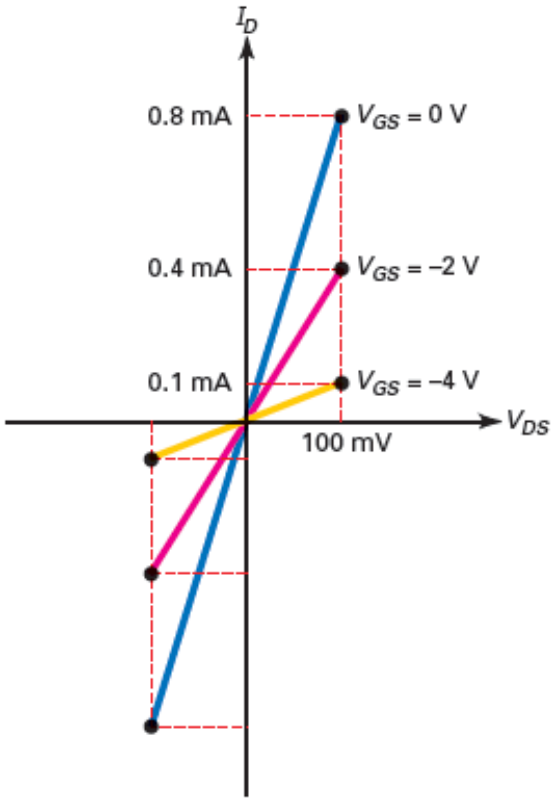


Figure-22 Small-signal r_{ds} is voltage controlled

- Recall that a JFET is a symmetrical device at low frequencies since either end can act like the source or the drain. This is why the drain curves of Figure-22 extend on both sides of the origin.
- This means that a JFET can be used as a voltage-controlled resistance for small ac signals, typically those with a peak-to-peak value of less than 200 mV. When it is used in this way, the JFET does not need a dc drain voltage from the supply because the small ac signal supplies the drain voltage.

1.11.6 Automatic Gain Control

- When a receiver is tuned from a weak to a strong station, the loudspeaker will blare (become loud) unless the volume is immediately decreased. The volume may also change because of fading, a decrease in signal caused by a change in the path between the transmitter and receiver.
- To prevent unwanted changes in the volume, most modern receivers use automatic gain control (AGC). Figure-23 illustrates the basic idea of AGC.

- An input signal V_{in} passes through a JFET used as a voltage-controlled resistance. The signal is amplified to get the output voltage V_{out}. The output signal is fed back to a negative peak detector.
- The output of this peak detector then supplies the V_{GS} for the JFET. If the input signal suddenly increases by a large amount, the output voltage will increase.
- This means that a larger negative voltage comes out of the peak detector. Since V_{GS} is more negative, the JFET has a higher ohmic resistance, which reduces the signal to the amplifier and decreases the output signal.
- On the other hand, if the input signal fades, the output voltage decreases and the negative peak detector produces a smaller output. Since V_{GS} is less negative, the JFET transmits more signal voltage to the amplifier, which raises the final output.
- Therefore, the effect of any sudden change in the input signal is offset or at least reduced by the AGC action.

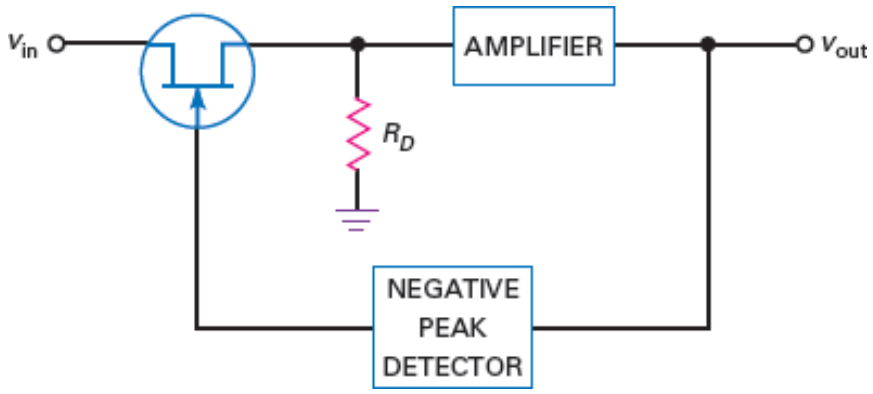


Figure-23 Automatic gain control

1.11.7 Cascode Amplifier

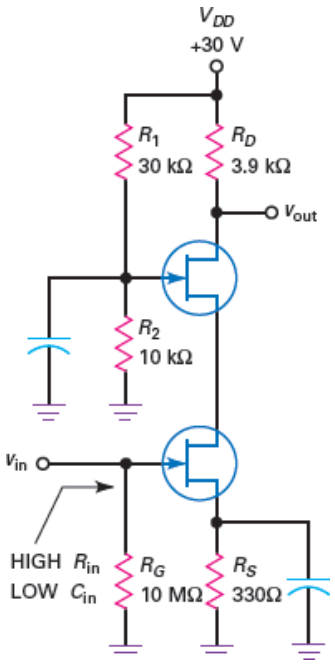


Figure-24 Cascode amplifier

- Figure-24 is an example of a cascode amplifier. It can be shown that the overall voltage gain of this two-FET connection is:

$$A_v = g_m r_d$$

- This is the same voltage gain as for a CS amplifier. The advantage of the circuit is its low input capacitance, which is important with VHF and UHF signals. At these higher frequencies, the input capacitance becomes a limiting factor on the voltage gain.
- With a cascode amplifier, the low input capacitance allows the circuit to amplify higher frequencies than are possible with only a CS amplifier.

1.11.8 Current Sourcing

- Suppose you have a load that requires a constant current. One solution is to use a shorted-gate JFET to supply the constant current. Figure-25a shows the basic idea. If the Q point is in the active region, as shown in Figure-25b, the load current equals I_{DSS}. If the load can tolerate the change in I_{DSS} when JFETs are replaced, the circuit is an excellent solution.

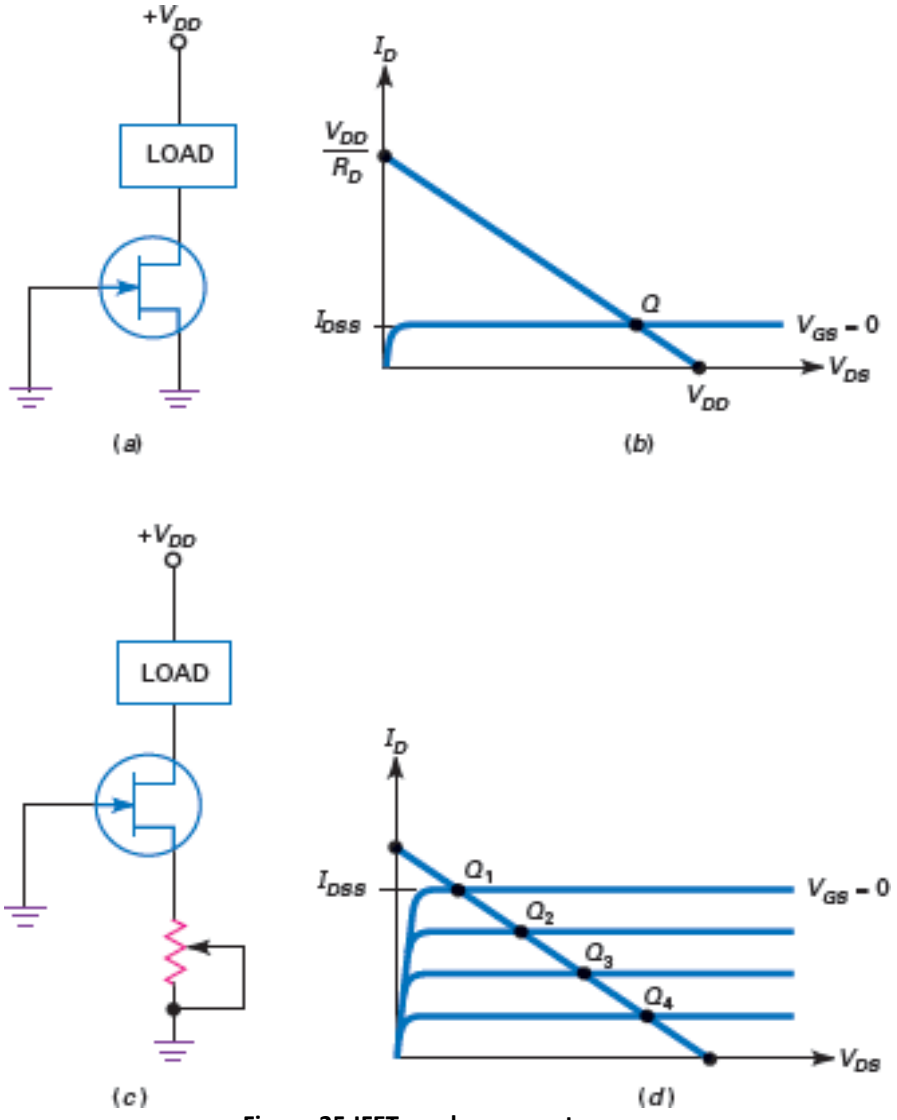


Figure-25 JFET used as current source

- On the other hand, if the constant load current must have a specific value, we can use an adjustable source resistor, as shown in Figure-25c. The self-bias will produce negative values of V_{GS}. By adjusting the resistor, we can set up different Q points, as shown in Figure-25d.
- Using JFETs like this is a simple way to produce a fixed load current, one that is constant even though the load resistance changes. In later chapters, we will discuss other ways to produce fixed load currents using op amps.

1.11.9 Current Limiting

- Instead of sourcing current, a JFET can limit current. Figure-26a shows how. In this application, the JFET operates in the ohmic region rather than the active region. To ensure operation in the ohmic region, the designer selects values to get the dc load line of Figure-26b.

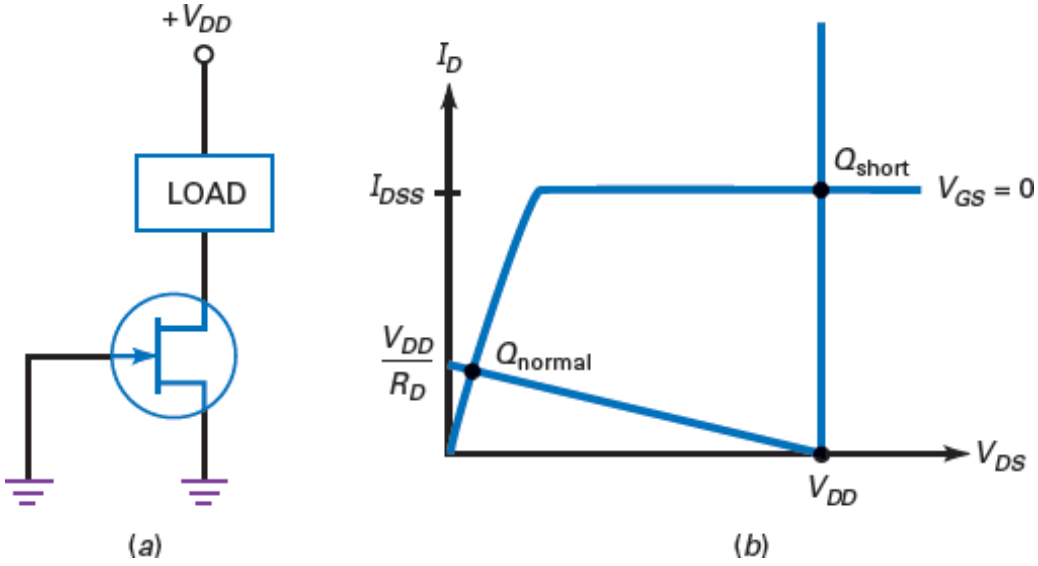


Figure-26 JFET limits current if load shorts

- The normal Q point is in the ohmic region, and the normal load current is approximately V_{DD}/R_D.
- If the load becomes shorted, the dc load line becomes vertical. In this case, the Q point changes to the new position shown in Figure-26b. With this Q point, the current is limited to I_{DSS}. The point to remember is that a shorted load usually produces an excessive current.
- But with the JFET in series with the load, the current is limited to a safe value.

1.12 MOSFETs

- The metal-oxide semiconductor FET, or MOSFET, has a source, gate, and drain. The MOSFET differs from the JFET, however, in that the gate is insulated from the channel. Because of this, the gate current is even smaller than it is in a JFET.
- There are two kinds of MOSFETs, the depletion-mode type and the enhancement-mode type. The enhancement-mode MOSFET is widely used in both discrete and integrated circuits.
- In discrete circuits, the main use is in power switching, which means turning large currents on and off. In integrated circuits, the main use is in digital switching, the basic process behind modern computers. Although their use has declined, depletion mode MOSFETs are still found in high-frequency front-end communications circuits as RF amplifiers.

1.13 The Depletion-Mode MOSFET

- Figure-27 shows a depletion-mode MOSFET, a piece of n material with an insulated gate on the left and a p region on the right. The p region is called the substrate.

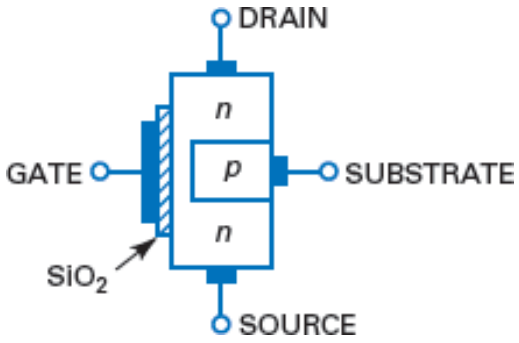


Figure-27 Depletion-mode MOSFET

- Electrons flowing from source to drain must pass through the narrow channel between the gate and the p substrate. A thin layer of silicon dioxide (SiO_2) is deposited on the left side of the channel.
- Silicon dioxide is the same as glass, which is an insulator. In a MOSFET, the gate is metallic. Because the metallic gate is insulated from the channel, negligible gate current flows even when the gate voltage is positive.
- Figure-28a shows a depletion-mode MOSFET with a negative gate voltage. The V_{DD} supply forces free electrons to flow from source to drain. These electrons flow through the narrow channel on the left of the p substrate.
- As with a JFET, the gate voltage controls the width of the channel. The more negative the gate voltage, the smaller the drain current. When the gate voltage is negative enough, the drain current is cut off. Therefore, the operation of a depletion-mode
- MOSFET is similar to that of a JFET when V_{GS} is negative. Since the gate is insulated, we can also use a positive input voltage, as shown in Figure-28b.
- The positive gate voltage increases the number of free electrons flowing through the channel. The more positive the gate voltage, the greater the conduction from source to drain.

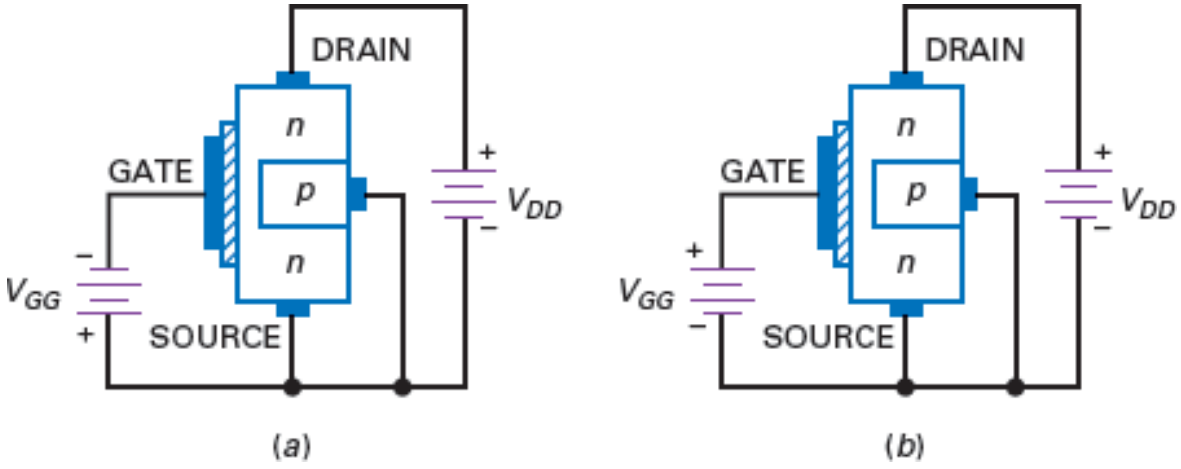


Figure-28 (a) D-MOSFET with negative gate; (b) D-MOSFET with positive gate

- There is also a p-channel D-MOSFET. It consists of a drain-to-source p-channel, along with an n-type substrate. Once again, the gate is insulated from the channel.
- The action of a p-channel MOSFET is complementary to the n-channel MOSFET. The schematic symbols for both n-channel and p-channel D-MOSFETs are shown in Figure-29.

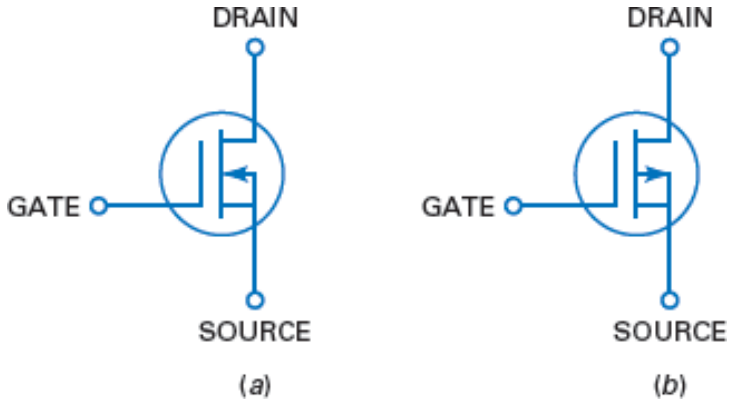


Figure-29 D-MOSFET schematic symbols: (a) n-channel; (b) p-channel

1.14 The Enhancement-Mode MOSFET

- The depletion-mode MOSFET was part of the evolution toward the enhancement mode MOSFET, abbreviated E-MOSFET. Without the E-MOSFET, the personal computers that are now so widespread would not exist.

1.14.1 The Basic Idea

- Figure-30a shows an E-MOSFET. The p substrate now extends all the way to the silicon dioxide. As you can see, there no longer is an n channel between the source and the drain. How does an E-MOSFET work? Figure-30b shows normal biasing polarities.

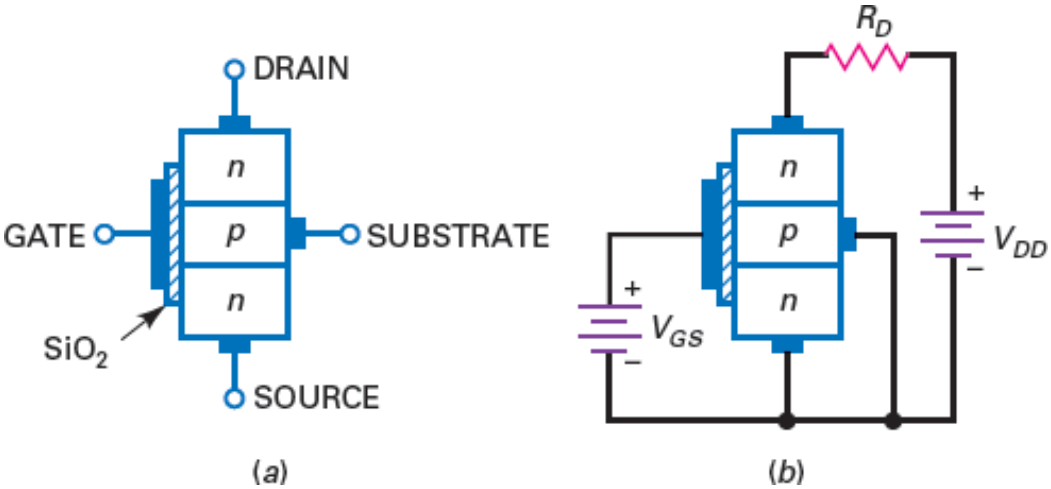


Figure-30 Enhancement-mode MOSFET: (a) Unbiased; (b) biased

- When the gate voltage is zero, the current between source and drain is zero. For this reason, an E-MOSFET is normally off when the gate voltage is zero.
- The only way to get current is with a positive gate voltage. When the gate is positive, it attracts free electrons into the p region.

- The free electrons recombine with the holes next to the silicon dioxide. When the gate voltage is positive enough, all the holes touching the silicon dioxide are filled, and free electrons begin to flow from the source to the drain.
- The effect is the same as creating a thin layer of n-type material next to the silicon dioxide. This thin conducting layer is called the n-type inversion layer. When it exists, free electrons can flow easily from the source to the drain.
- The minimum V_{GS} that creates the n-type inversion layer is called the threshold voltage, symbolized by $V_{GS(th)}$. When V_{GS} is less than $V_{GS(th)}$, the drain current is zero.
- When V_{GS} is greater than $V_{GS(th)}$, an n-type inversion layer connects the source to the drain and the drain current can flow. Typical values of $V_{GS(th)}$ for small-signal devices are from 1 to 3 V.
- The JFET is referred to as a depletion-mode device because its conductivity depends on the action of depletion layers. The E-MOSFET is classified as an enhancement-mode device because a gate voltage greater than the threshold voltage enhances its conductivity.
- ***With zero gate voltage, a JFET is on, whereas an E-MOSFET is off. Therefore, the E-MOSFET is considered to be a normally off device.***

1.14.2 Schematic Symbol

- When $V_{GS} = 0$, the E-MOSFET is off because there is no conducting channel between source and drain. The schematic symbol of Figure-31a has a broken channel line to indicate this normally off condition.
- As you know, a gate voltage greater than the threshold voltage creates an n-type inversion layer that connects the source to the drain.
- The arrow points to this inversion layer, which acts like an n channel when the device is conducting.
- There is also a p-channel E-MOSFET. The schematic symbol is similar, except that the arrow points outward, as shown in Figure-31b.
- The p-channel E-MOSFET is also a normally off enhancement-mode device. To turn on a p-channel E-MOSFET, the gate must be made negative with respect to the source.
- The $-V_{GS}$ value must reach or exceed the $-V_{GS(th)}$ value for conduction. When this occurs, a p-type inversion layer is formed with holes being the majority carriers.
- The n-channel E-MOSFET uses electrons as the majority carriers which have higher mobility than the p-channel holes. This results in a lower $R_{DS(on)}$ and higher switching speeds for the n-channel E-MOSFET.

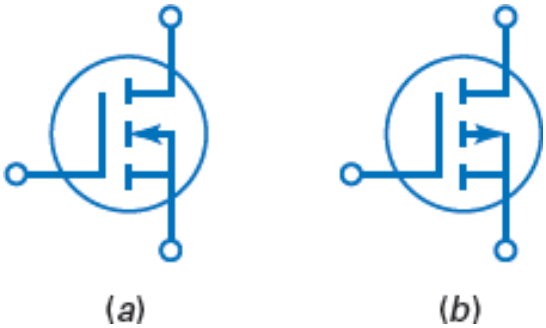


Figure-31 EMOS schematic symbols: (a) N-channel device; (b) p-channel device

Unit 5: Field effect transistors (FET) and its Biasing

1.15 CMOS

- With active-load switching, the current drain with a low output is approximately equal to $I_{D(sat)}$. This may create a problem with battery-operated equipment.
- One way to reduce the current drain of a digital circuit is with complementary MOS (CMOS). In this approach, the IC designer combines n-channel and p-channel MOSFETs.
- Figure-32a shows the idea. Q_1 is a p-channel MOSFET and Q_2 is an n-channel MOSFET. These two devices are complementary; that is, they have equal and opposite values of $V_{GS(th)}$, $V_{GS(on)}$, $I_{D(on)}$, and so on.
- The circuit is similar to a Class-B amplifier because one MOSFET conducts while the other is off.

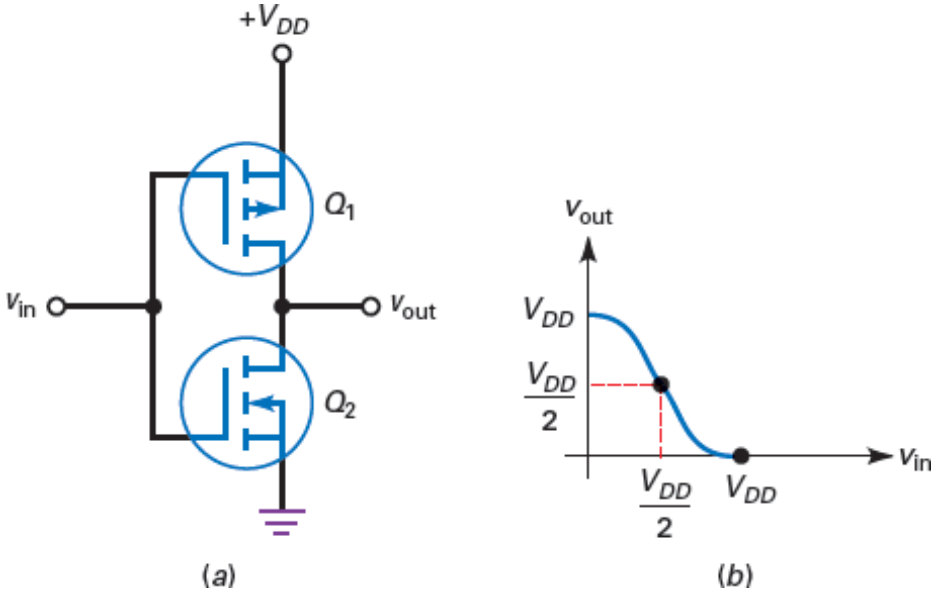


Figure-32 CMOS inverter: (a) Circuit; (b) input-output graph

1.15.1 Basic Action

- When a CMOS circuit like Figure-32a is used in a switching application, the input voltage is either high (+V_{DD}) or low (0 V). When the input voltage is high, Q_1 is off and Q_2 is on. In this case, the shorted Q_2 pulls the output voltage down to ground.
- On the other hand, when the input voltage is low, Q_1 is on and Q_2 is off. Now, the shorted Q_1 pulls the output voltage up to +V_{DD}. Since the output voltage is inverted, the circuit is called a CMOS inverter.
- Figure-32b shows how the output voltage varies with the input voltage. When the input voltage is zero, the output voltage is high. When the input voltage is high, the output voltage is low.
- Between the two extremes, there is crossover point where the input voltage equals V_{DD}/2. At this point, both MOSFETs have equal resistances and the output voltage equals V_{DD}/2.

1.15.2 Power Consumption

- The main advantage of CMOS is its extremely low-power consumption. Because both MOSFETs are in series in Figure-32a, the quiescent current drain is determined by the non-conducting device.

- Since its resistance is in the mega-ohms, the quiescent (idling) power consumption approaches zero. The power consumption increases when the input signal switches from low to high, and vice versa.
- The reason is this: At the midway point in a transition from low to high or vice versa, both MOSFETs are on. This means that the drain current temporarily increases.
- Since the transition is very rapid, only a brief pulse of current occurs. The product of the drain supply voltage and the brief pulse of current means that the average dynamic power consumption is greater than the quiescent power consumption.
- In other words, a CMOS device dissipates more average power when it has transitions than when it is quiescent. Since the pulses of current are very short, however, the average power dissipation is very low even when CMOS devices are switching states.
- In fact, the average power consumption is so small that CMOS circuits are often used for battery-powered applications such as calculators, digital watches, and hearing aids.

1.16 E-MOSFET Amplifiers

- As mentioned in previous sections, the E-MOSFET finds its use primarily as a switch. Applications do exist for this device to be used as an amplifier, however.
- These applications include front-end high-frequency RF amplifiers used in communications equipment and power E-MOSFETs used in Class-AB power amplifiers.
- With E-MOSFETs, V_{GS} has to be greater than $V_{GS(th)}$ for drain current to flow. This eliminates self-bias, current-source bias, and zero bias because all these will have depletion-mode operation.
- This leaves gate bias and voltage-divider bias. Both of these biasing arrangements will work with E-MOSFETs because they can achieve enhancement-mode operation.
- Figure-33 shows the drain curves and the transconductance curve for an n-channel E-MOSFET. The parabolic transfer curve is similar to that of D-MOSFET with some important differences.

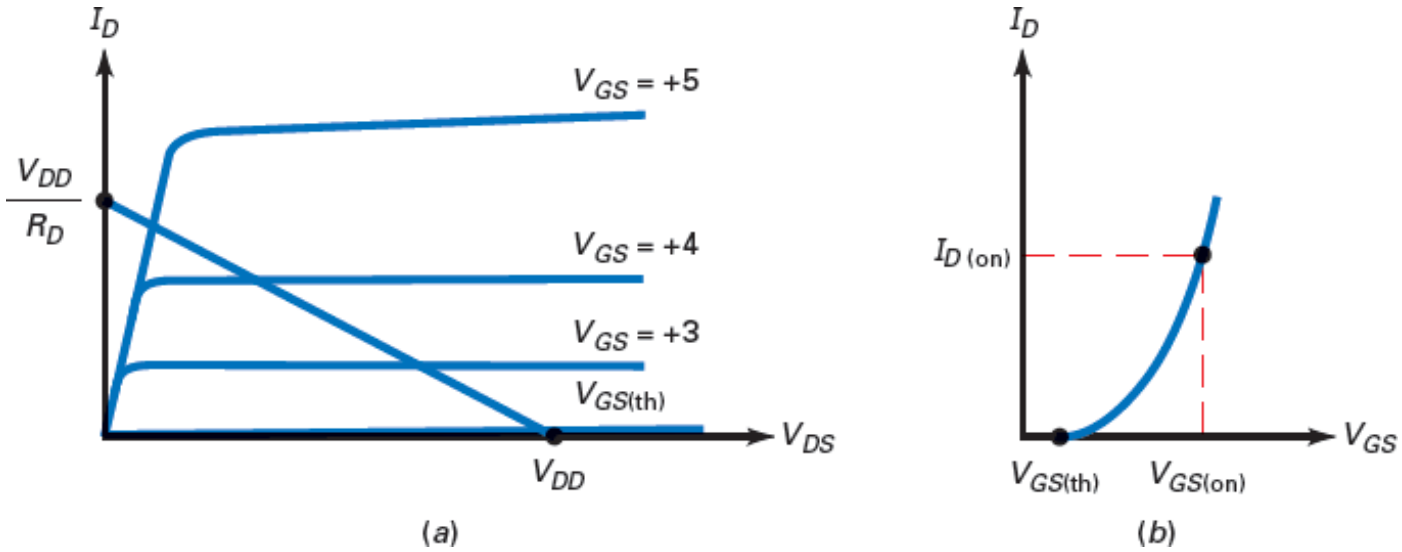


Figure-33 An n-channel E-MOSFET: (a) Drain curves; (b) transconductance curve

- The E-MOSFET operates only in the enhancement mode. Also, the drain current doesn't start until $V_{GS} = V_{GS(th)}$.

- Again, this demonstrates that the E-MOSFET is a voltage-controlled normally off device. Because the drain current is zero when $V_{GS} = 0$, the standard transconductance formula will not work with the E-MOSFET.
- The drain current can be found by:

$$I_D = k[V_{GS} - V_{GS(th)}]^2 \quad \text{---------- (25)}$$

Where k is a constant value for the E-MOSFET found by:

$$k = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2} \quad \text{---------- (26)}$$

- Figure-34a shows another biasing method for E-MOSFETs called drain-feedback bias. This biasing method is similar to collector-feedback bias used with bipolar junction transistors.
- When the MOSFET is conducting, it has a drain current of $I_{D(on)}$ and a drain voltage of $V_{DS(on)}$. Because there is virtually no gate current, $V_{GS} = V_{DS(on)}$. As with collector-feedback, drain-feedback bias tends to compensate for changes in FET characteristics.
- For example, if $I_{D(on)}$ tries to increase for some reason, $V_{DS(on)}$ decreases. This reduces V_{GS} and partially offsets the original increase in $I_{D(on)}$.
- Figure-34b shows the Q point on the transconductance curve. The Q point has the coordinates of $I_{D(on)}$ and $V_{DS(con)}$. Data sheets for E-MOSFETs often give a value of $I_{D(on)}$ for $V_{GS} = V_{DS(on)}$.

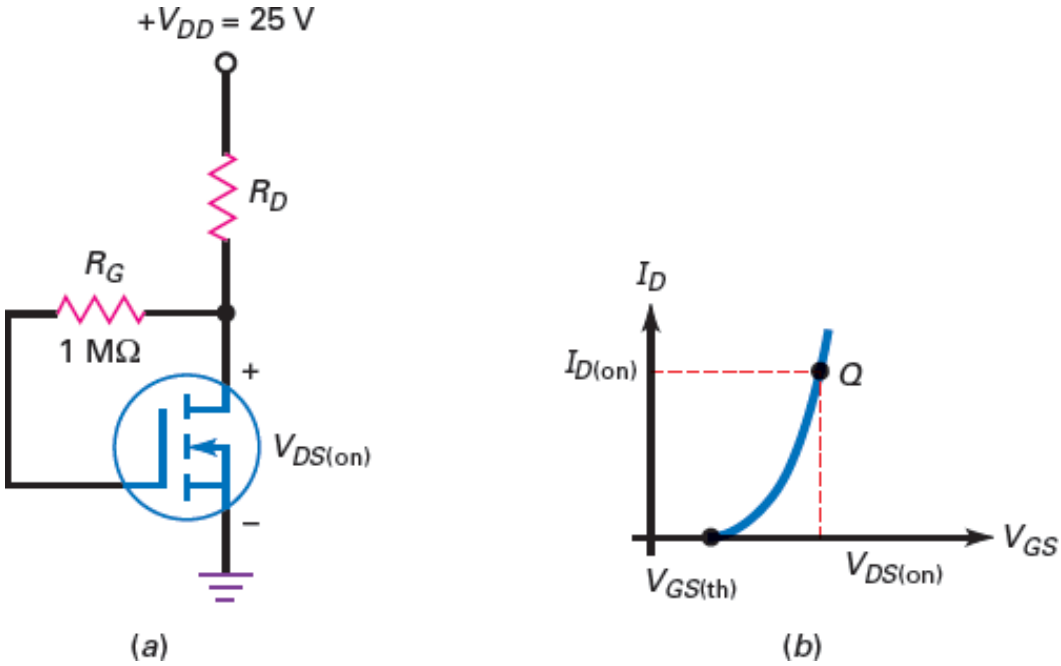


Figure-34 Drain-feedback bias: (a) Biasing method; (b) Q point

- When designing this circuit, select a value of R_D that produces the specified value of V_{DS}. This can be found by:

$$R_D = \frac{V_{DD} - V_{DS(on)}}{I_{D(on)}} \quad \text{---------- (27)}$$

- The transconductance value will vary, depending on the circuit's Q point, following the relationship of $I_D = k[V_{GS} - V_{GS(th)}]^2$ and $g_m = \frac{\Delta ID}{\Delta V_{GS}}$ ---------- (28)

1.17 MOSFET Testing

- MOSFET devices require special care when being tested for proper operation. As stated previously, the thin layer of silicon dioxide between the gate and channel can be easily destroyed when V_{GS} exceeds $V_{GS(max)}$.
- Because of the insulated gate, along with the channel construction, testing MOSFET devices with an ohmmeter or DMM is not very effective. A good way to test these devices is with a semiconductor curve tracer.
- If a curve tracer is not available, special test circuits can be constructed. Figure-35 shows a circuit capable of testing both depletion-mode and enhancement-mode MOSFETs. By changing the voltage level and polarity of V_1, the device can be tested in either depletion or enhancement modes of operation.

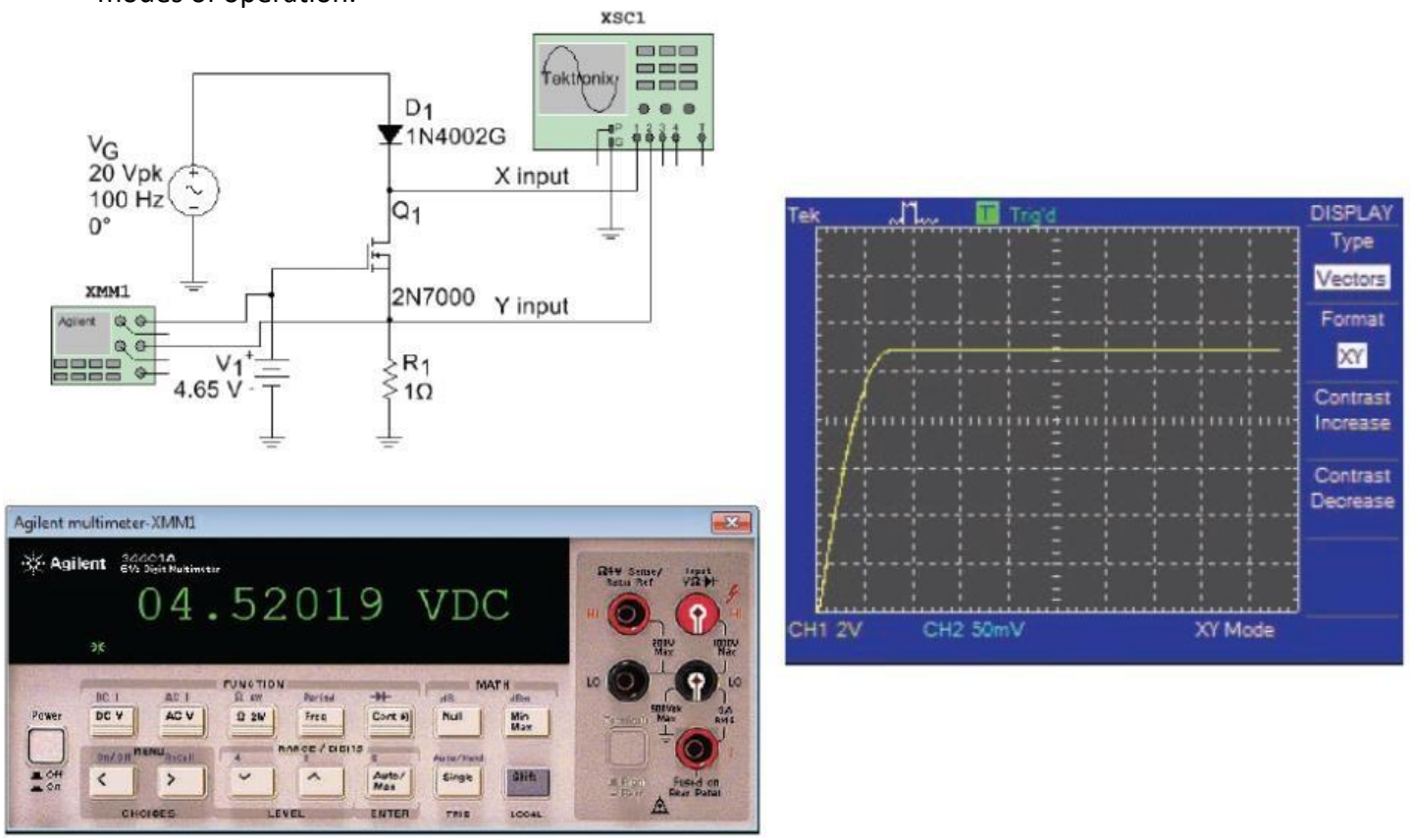


Figure-35 MOSFET testing

- The drain curve shown in Figure-35 shows the approximate drain current of 275 mA when, V_{GS} = 4.52 V. The y-axis is set to display 50 mA/div.
- An alternative to the aforementioned testing methods is to simply use component substitution. By measuring in-circuit voltage values, it is often possible to deduct that the MOSFET is defective. Replacing the device with a known good component should lead you to a final conclusion.

Unit 5: Field effect transistors (FET) and its biasing